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Processing Materials Devices and Diagnostics for Thin Film Photovoltaics: Fundamental and Manufacturability Issues

Final Report
1 March 2005 – 30 November 2008

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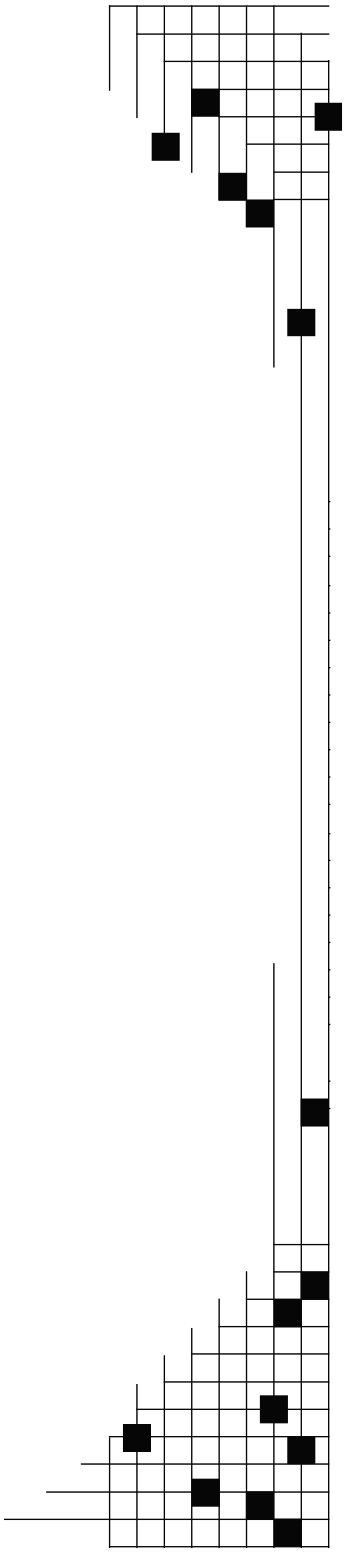

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Abstract

This report describes results achieved under this subcontract to develop and understand thin film solar cell technology associated to $CuInSe_2$ and related alloys, a-Si and its alloys and CdTe. This includes application of a-Si to c-Si wafer-type cells as well. Modules based on all these thin films are promising candidates to meet DOE long-range efficiency, reliability and manufacturing cost goals. The critical issues being addressed under this program are intended to provide the science and engineering basis for the development of viable commercial processes and to improve module performance. The generic research issues addressed are: 1) quantitative analysis of processing steps to provide information for efficient commercial scale equipment design and operation; 2) device characterization relating the device performance to materials properties and process conditions; 3) development of alloy materials with different bandgaps to allow improved device structures for stability and compatibility with module design; 4) development of improved window/heterojunction layers and contacts to improve device performance and reliability; and 5) evaluation of cell stability with respect to illumination, temperature and ambient and with respect to device structure and module encapsulation.

1 OBJECTIVES, TRAINING, AND PUBLICATIONS

The primary objectives of the NREL-sponsored research at the Institute of Energy Conversion (IEC) research are listed below according to the specific 3 types of thin film solar cells currently under commercial interest. In addition, generic process diagnostic and control tools will be developed. Student training and publication statistics are also summarized.

1.1 CdTe/CdSe-based Solar Cells

The CdTe effort will address increased voltage and stability, the development of an in-line CdTe process to implement high rate and high throughput deposition on a moving substrate, and fundamental studies of CdTe surface chemistry. To meet these objectives, IEC will:

- Separate and quantify the effect on V_{OC} of high resistance (HR) buffer layers such as Ga_2O_3 and In_2O_3 and widening the CdS window layer bandgap with Zn.
- Develop and apply a transparent back contact to CdTe to probe back contact junction formation and degradation.
- Evaluate methods for increasing V_{OC} by reducing space charge recombination.
- Conduct detailed analysis of collection losses using conventional and bifacial devices, AMPS modeling, and JV measurements under different conditions.
- Improve the stability of CdTe devices by developing alternative processing steps to 'stabilize' the junction and contact; and to compare the effects of well-controlled stress conditions on CdTe solar cells by performing detailed device analysis and relating results to differences in fabrication.
- Develop the fundamental understanding needed for high throughput CdTe module fabrication by controlling high rate delivery of Cd and Te species to the moving substrate surface.
- Develop rapid and reproducible post-deposition processing alternatives to the current $CdCl_2$ vapor treatment.
- Determine fundamental understanding of etching and wet processing steps on CdTe surfaces
- Determine relation between the contact processing and CdTe surface chemistry, and the device performance and stability especially as applies to First Solar devices.

1.2 $CuInSe_2$-based Solar Cells

The $CuInSe_2$-based effort will characterize fundamental properties of interfaces in $CuInSe_2$-based solar cells, develop approaches to improving V_{OC} including alloying with S and Al, and will also include the development of an in-line process for deposition on a moving substrate. To meet these objectives, IEC will:

- Develop the in-line deposition of $Cu(InGa)Se_2$ films from stationary elemental evaporation sources onto moving rigid (Mo coated glass) and flexible (Mo coated polyimide) substrates at rates commensurate with commercial manufacturing.

- Determine the relationship of the film properties, both compositional and structural, to the solar cell performance with particular emphasis on the effect of complex band-gap profiles due to the depth distribution of Ga and In and incorporation of Na.

- Increase the operating voltage by increasing the bandgap, E_g, in the absorber layer or in the space charge region using $Cu(InAl)Se_2$ alloys.

- Investigate the feasibility of controlled p–type doping of the $Cu(InGa)Se_2$ or $Cu(InAl)Se_2$ absorber layers to increase V_{OC}.

- Provide a fundamental understanding of surface reactions and interface chemistry in the fabrication of CIGS devices using atomic level surface characterization techniques to study the Mo surface, Mo/ $Cu(InGa)Se_2$ interface, the free $Cu(InGa)Se_2$ surface and $Cu(InGa)Se_2$/CdS interface.

- Determine reaction pathways for the formation of $Cu(InGa)Se_2$ and $Cu(InGa)(SeS)_2$ on H_2Se/H_2S time-temperature-gas concentration profiles using sputtered Cu/Ga/In precursors.

- Fabricate devices with CdS, ZnS, and CdZnS buffer layers and $CuInSe_2$ with Ga, S, and/or Al alloy absorber layers in order to characterize the effect buffer layers on device behavior and fundamental interface properties.

1.3 Si-based Solar Cells

The Si-based effort will focus on developing a process for fabricating polycrystalline Si solar cells and materials at low temperatures on low cost substrates as well as the use of microcrystalline Si layers in solar cells. To meet these objectives, IEC will:

- Develop in-situ and/or post-deposition methods such as metal induced crystallization (MIC) to produce HWCVD deposited Si films and devices with grains in the micrometer range.

- Investigate various forms of Eutectic Promoted Deposition (EPD) where very thin metal layers deposited on glass substrates are briefly heated above the metal-Si eutectic as the HWCVD Si deposition proceeds leading to precipitation of Si from the supersaturated liquid solution.

- Investigate the feasibility of layer-by-layer deposition (LBL) to create thin Si seed layers in-situ to enhance nucleation of larger grains during subsequent growth.

- Develop all HWCVD p n junction devices by developing HWCVD emitter layers on large grain HWCVD absorbers.

- Develop processing of c-Si heterojunction solar cells using PECVD deposited emitters and contacts with increased V_{OC}.

- Investigate alternative contact structures for c-Si solar cells utilizing improved passivation.

- Investigate chemical surface treatments leading to high effective lifetimes.

- Develop texturing approaches compatible with effective passivation.

1.4 In-line Diagnostics

The in-line process diagnostic effort will develop diagnostic tools needed for process control and the associated quantitative models that link sensor outputs to process variables and material properties. To meet these objectives, IEC will:

- Understand the fundamentals of thin film growth and identification of critical properties that lead to efficient solar cells, i.e., product specifications.

- Identifying process parameters, to which film properties are sensitive, i.e., process determinants.

- Develop robust, reliable and fast-response sensor equipment for in-situ applications in deposition reactors.

- Develop quantitative models that relate sensor output to process determinants and film properties for use in model based process control, i.e., intelligent process control.

1.5 Training and Education

During the period of this subcontract (September 5, 2001 to May 31, 2008) IEC provided training and education for the following: 7 visiting professionals, 2 of which were Fulbright scholars; 20 post-doctoral fellows/limited term researchers; 25 graduate students; and 33 undergraduate students. A complete list of names is given in the list of contributors.

1.6 Publications

As a result of research performed under this contract, IEC published 140 papers. See the complete list under Section 6.

1.7 Thin Film Partnership (TFP) Team Activities and Collaborations

Since IEC was a major contributor to the NREL Thin Film Partnership (TFP) Teams, our collaborations and activities in this area are discussed in each Phase for each of the three teams (CdTe, Cu(InGa)Se2, and Amorphous and Thin Si). IEC staff served as Leaders of various sub-teams within each of the above teams. Reviews of various topics of interest were prepared and presented at the team meetings. The considerable collaborations between IEC with other universities and industrial groups resulted in publications, demonstrated improvements in technology, and mutual benefit to National Thin Film Partnership. Several graduate students who received their training at IEC funded by the TFP are now working in the US PV industry.

1.8 Organization of the Report

This report contains the summary of results from the first 6 Phases of this contract. They are each organized into four technical sections: CdTe-based solar cells, $CuInSe_2$-based solar cells, Si-based solar cells, and In-line Process Diagnostics. More complete details can be found in the Annual Reports for each phase which are posted on the IEC website whose link is given. Following the summary of each previous Phase, detailed results from the final Phase, January 01, 2008 to May 31, 2008 is given.

2 CdTe-BASED SOLAR CELLS

2.1 Phase 1 Summary: 9/5/01 to 9/4/02

The influence of the high resistance (HR) layer and CdS layer was studied using detailed analysis of J(V) measurements. A series of devices were fabricated with 40 or 80 nm of Ga_2O_3 or In_2O_3 HR layers having 0 or 80 nm CdS. Cells without CdS had V_{oc}~0.1-0.2 V and very large voltage dependent photocurrent suggesting a very low built in field. Reverse bias of –2V was needed to saturate the QE of cell without CdS. Analysis of temperature and intensity dependent J(V) and $V_{oc}(T)$ showed that devices with CdS have much higher A factors compared to CdS-free devices (1.6-2.0 compared to 1.1-1.2) and 4 orders of magnitude lower J_o. The activation energy for recombination ϕ /A was obtained from an Arrhenios plot of J_o where ϕ should equal the bandgap for SRH recombination . Values of ϕ/A for 0 and 80 nm CdS were 0.54 and 0.73 eV, respectively. The value of ϕ/A=0.73 eV is near mid gap consistent with the A factors close to 2. This indicates the CdS devices are limited by SRH type recombination but the CdS-free devices are limited by a different mechanism. The intercepts of V_{oc} vs T are ϕ/q ~1.4 V and ~0.6 V for CdS and CdS-free devices. This confirms that the CdS device has SRH recombination since the intercept ϕ =Eg of CdTe. The CdS-free device has a much lower barrier which explains the poor voltage dependent collection hence low FF and a different recombination mechanism (A~1) than CdS devices (A~2). One possibility is interface recombination. No clear difference between In_2O_3 or Ga_2O_3 was found.

The effects of adding extra Cu into the cell structure to simulate the high Cu throughout the cell structure, as may occur during device stressing, was studied. Devices were processed with thin Cu films deposited between either the ITO and CdS layers or between the CdS and CdTe layers, and contacts were deposited following IEC's baseline recipe. Initial results showed devices with extra Cu films all exhibited low V_{oc}, attributed to high doping of the cell junction region, and strong J-V rollover compared to control cells. Cu was observed to diffuse to the back (CdTe) surface of the cell during processing, so the presence of Cu oxides at the back surface may account for the observed rollover. Structural investigations also determined changes in CdS crystal structure when deposited on Cu films compared to CdS deposited on ITO. Later studies to isolate the cause of rollover in the cells were hindered by shunting and poor adherence of the CdTe/CdS layers. QE measurements on the initial set of cells showed that the presence of the thin Cu films in the cell structure had a profound effect on the photocarrier recombination and transport with some similarities to Cu-sensitized photoconductive CdS and suggests that much smaller amounts of Cu present in the cell structure could lead to degradation in device behavior.

The possibility of photoconductive CdS was studied further using the bias light spectrum of QE. An enhancement of the blue response by red bias light was found in devices from BP Solar, First Solar, and Institute of Energy Conversion. The effect becomes more pronounced after stress, and at MP more than SC. The QE can easily exceed unity

indicating this is a secondary photoconductive effect. No such effect was seen for CdS-free devices. This gives motivation for further study of Cu-doped CdS since it may give insight into stress-related degradation.

With stress, Cu_2Te back contacts on CdTe/CdS solar cells have been previously observed to transform to the less favorable CuTe species (an oxidation process). A new approach to stabilizing back contacts was begun using additives in the back contact paste to preserve the Cu_2Te back contact by surface complexation or redox chemistry. Cells were prepared containing a range of additives, including a number of complexing and reducing agents, in the carbon paste contact. Initial device processing determined that complexing agents scavenged Cu from the back contacts, which resulted in poor performance (either initially following contact processing or following short thermal stress) including significant J-V rollover. Cells contacted with pastes containing reducing agents showed, with stress, an attenuation of the formation of J-V rollover compared to control cells. These results highlight that CdTe/CdS device performance can be significantly affected by the presence of a small amount of chemically active species in the back contact. Attempts to stabilize back contacts by using Cu compounds and complexes as additives in the paste as both the source of Cu and the stabilizing species were not successful. However, these results highlighted that Cu powder and Cu(I) salts (e.g. CuCl, CuI) could form a favorable back contact, whereas, due to their higher stability, Cu(II)-complexes could not.

An investigation of the action of NP and Br_2-meth etching on CdTe has been carried out. Variable Angle Spectroscopic Ellipsometry (VASE) and Glancing Incidence X-ray Diffraction (GIXRD) were applied to investigate effects of etching on CdTe surfaces. It was found that etching in 1% NP (NP1) for >40s resulted in the formation of relatively thick crystalline Te surface layers. With shorter times, the initial Te surface layer contained a higher degree of amorphous phase which spontaneously crystallizes over time following removal from the etch solution. In contact with ambient atmospheric conditions, the NP etched surface was stable to oxidation for ~3-4 h. By comparison, Br_2-meth etching produces a very thin Te-rich layer on CdTe, which begins to oxidize immediately following removal from solution. As NP etching proceeds, bubbling (NO(g) or NO_2(g)) begins on the CdTe surface. The commencement of bubbling coincides with significant formation and consumption of Te.

GB etching can be a problem associated with cells that have received NP etching. We have attempted to adjust the NP etch properties to reduce effects of GB etching. The initial approach was to increase the acidity of the etch solution, to allow fast formation of the Te surface layer over very short immersion times. Higher acidity etches could produce surface levels of Te similar to NP1 following just 2-6s immersion. SEM confirmed no GB widening had occurred at these times, but did occur at immersion times >8s. Test-tube reactions also suggest that the higher acidity etches may proceed via a different mechanism.

A further approach to slowing GB etching is the use of high viscosity etch solutions. An investigation of the effect of using solutions of varying viscosity on the action of Br_2 on

CdTe surfaces has begun. Increasing solvent viscosity will slow the rate of GB diffusion of the etchant. AFM and VASE measurements indeed show that the rate of CdTe etching is slowed in etch solutions prepared with higher viscosity solvents.

There is a clear need to establish better correlation between accelerated stressing performed in the lab and conditions experienced in the field. Typically, lab stressing has been done at 70-100°C in a continuous manner while modules in the field see temperatures from 20-60°C with cyclic (daily) light exposure and power generation. It is possible that some relaxation effects might occur during the dark portion of the cycle which would result in lower or negligible degradation for cyclically stressed devices. Therefore, we designed a series of stress experiments with various cycles of light (L), dark (D) and temperature (65° or 20°C). Two sets of BP and FS devices (i.e. with their own contact) were stressed at each of the above conditions for 30 days. In each stress, there was one at OC and at 1/2 OC bias. V_{oc} was monitored at 65°C after the 8 or 16 hours of dark and 16 or 8 hours of light to see if there was any relaxation or recovery after short periods of darkness. A key result, identified for the first time, is that V_{oc} after daily OC stressing in both FS and BP devices can show a daily variation, repeated every day for 30 days. We observed a 30-50 mV recovery in V_{oc} during 16 hours of darkness, followed by 30-50 mV decrease in V_{oc} during 8 hours illumination. Degradation with stress for FS or BP cells is not simply correlated to the exposure time. For FS devices, the stability is strongly bias dependent. Bias at 1/2 OC is nearly stable while OC is very unstable. One type of FS devices shows recovery of ~50 mV in V_{oc} with nightly periods of dark while the other does not. We also analyzed the dark JV curves of the FS devices. Before stress, we found typically A=1.5, R_s=4-5 Ω-cm^2, and J_o=1E-10 A/cm^2. After stress, we found differences depending on the bias during stress, but not so clearly on the stress cycle. FS cells stressed at OC showed: an increase in A factor from 1.5 to 1.9, no change in R_s, and either a decrease or increase in J_o of 10-100X. We have never before seen a decrease in J_o with stress on FS devices, but this is consistent with the increase in V_{oc} of 30-60 mV. No blocking contact was observed in the dV/dJ plots. In contrast to FS, stability in BP devices has a very weak bias dependence, instead correlating with time at 65°C more than bias. They also show partial recovery in V_{oc}~30 mV overnight and nearly complete recovery after a week in the dark at room temperature. Degradation is nearly all in V_{oc}. Analysis of J(V) curves for BP devices showed a consistent increase in A factors from 1.9 to 2.2 and in J_o from 1E-9 to 2E-8 A/cm$_2$ with stress. There was no significant increase in R_s and no blocking contact curvature observed after stress.

The properties of vapor transported CdTe films deposited onto moving CdS/ITO/glass superstrates were determined for different deposition temperatures and growth ambients. A vapor transport deposition (VTD) system was used to deposit onto a 10 cm wide translating substrate at temperatures from 450°C to 550°C. For depositions in pure He, the roughness increased with substrate temperature and film texture changed from (111) at low temperature to (220) at high temperature. Deposition in He+O_2 ambient produced smoother films, even at greater film thickness, with near-random texture. Unlike PVD films, which exhibit in-plane compressive strain, the lattice parameter in VTD films is equal to that for pure unstrained CdTe. The VTD films exhibit a sharp optical absorption edge with 60-70% sub-band gap absorption.

A first-order model for VTD radiative transfer within the source and for VTD CdTe film deposition with a carrier gas was developed. CdTe films were deposited at ~1 μm/min static equivalent deposition rate onto CdS/ITO/glass superstrates translating 1 cm/min beneath the source. The radiative model was used to optimize the filament geometry within the source. The mass transfer model and measured source effusion verify that the source operates by saturation of the carrier gas with Cd and Te_2 vapor. CdTe/CdS devices were fabricated using VTD CdTe films deposited at different substrate temperatures and ambient to establish baseline conditions. This has yielded cells with ~11% efficiency for deposition at 550°C in $He+O_2$ ambient. Deposition at higher substrate temperature onto window layers incorporating high resistance buffer layers is expected to yield high conversion efficiency devices to serve as a baseline for further optimization.

CdTe TFP Team Activity and Collaboration

IEC attended the 14th CdTe TFP Team Meeting, held at the Florida Solar Energy Center in Cocoa, Florida. We made presentations on results of activity in three sub-teams, and on cyclic stressing of CdTe devices, as detailed below. Detailed results are presented in the CdTe Team Minutes.

Stressing Sub-team

Considerable work involving cyclic stressing was performed on BP and FS samples. Some was reported in the Annual Report, at the 14th CdTe TFP Team Meeting, and privately to the two companies.

Micrononuniformity sub-team

First Solar provided various groups with pieces in unstressed and stressed condition. We analyzed cells from pieces FS-B11080213-K4B (unstressed) and -K5A (stressed). We found that with stress, the diode recombination J_o increases by 3-4 orders of magnitude from ~$1x10^{-10}$ to $1x10^{-6}$ mA/cm^2 and A increases from 1.6 to 2.0. The series resistance increased from 3 to 6 Ω-cm^2 and blocking contact behavior appeared. The intercept of V_{oc} vs. T decreased from 1.53 to 1.48 eV. These results are very consistent with other results we have obtained from FS devices over the years either with their contact (like these) or with IEC contact, which had been stressed either at FS or at IEC.

We also analyzed sputtered CdTe devices from University of Toledo having Cu/Au contacts. Piece 971B was in the initial state and 966C was stressed. Stressing was performed at UT for 27 days at 60°C at 1 sun at OC. UT provided us with their JV data. We found that the stressed devices had recovered in V_{oc} and FF in the month between testing at UT and at IEC. Efficiency was ~11.6% initial and ~11.2% stressed. This represents surprisingly good stability for Cu/Au contacts. Devices had curvature in dV/dJ even in initial state. Series resistance increased from 2 to 4 Ω-cm^2 and J_0 increased from $1x10^{-7}$ to $3x10^{-6}$ mA/cm^2 with stress. CV under different bias light conditions indicated

the CdTe is completely depleted even at 0V in the light, suggesting a carrier density less than $1x10^{14}$ cm^{-3}. This is similar to BP devices. In contrast, FS devices require –3 V for depletion and have carrier densities of ~$5x10^{14}$ cm^{-3}. Carrier density decreases with stress in FS devices.

We summarize our findings for FS, BP and UT devices regarding grain size, stability, dark recovery, carrier density, and deposition methods. We note the following correlation: BP and UT devices have small grains and similar stability and carrier density despite having very different deposition and contact processing. FS devices, measured so far, have larger grains, poorer stability, very strong bias dependence to stressing, and higher carrier density.

$CdCl_2$ Sub-Team

A post deposition treatment matrix was employed to systematically determine the role of $CdCl_2$ and air processing on electrodeposited films supplied by BP Solar and PVD films supplied by Canrom. For the BP Solar CdTe/CdS, cells were fabricated using CdTe/CdS from a single Apollo plate (3144) by varying treatment ambient, temperature, and time. AFM and GIXRD were used to characterize the film morphology and phase content prior to contacting. Back contacts were fabricated using the Cu-diffusion process, with Acheson 505SS C ink conductor. For cells with no treatment at all, low photocurrent was obtained. For single-step air heat treatments, J_{sc} <15 mA/cm^2 were obtained with V_{oc} < 700 mV. For single-step $CdCl_2$:Air vapor treatments, higher photocurrents, J_{sc} ~ 20 mA/$cm^{2,}$ were obtained, but again with V_{oc} < 700 mV. Combining the two treatments, air treatment at 450°C followed by $CdCl_2$: Air vapor treatment yielded J_{sc} ~ 20 mA/cm^2 and V_{oc} >700 mV. These results are qualitatively similar to those found for PVD films. The best cells had efficiency >11%.

For the Canrom CdTe/CdS, a small set of samples was surveyed using single-step $CdCl_2$:Air treatment and two-step treatment, with either a 600°C anneal in argon, or 450°C air treatment prior to the $CdCl_2$:Air treatment. For this material, the best cells had 7% efficiency, obtained with the single-step treatment in $CdCl_2$:Air. Surprisingly, the two-step processes yielded efficiencies less than 6%, suggesting that the higher temperatures may electrically activate an unknown contaminant in the structures.

Capacitance Sub-Team

Measurements of C(V) under various bias light conditions were performed on FS, BP and UT devices in initial and stressed states. Significant differences were observed in C-V behavior. Results were presented at the March 2002 Team Meeting and published in the minutes.

2.2 Phase 2 Summary: 9/5/02 to 9/4/03

Investigations of the dynamics of CdTe etching have continued. Variable Angle Spectroscopic Ellipsometry (VASE) has shown that bromine-methanol (BM) etching to be consistent and very reproducible. BM polishing of CdTe will be used for sample preparation for a systematic investigation of nitric-phosphoric (NP) etching of CdTe, to accurately determine Te thickness.

A number of devices, contacted with Cu-containing graphite paste, were prepared to monitor the effects of different etch treatments on cell performance and stability. Devices processed from Br_2-based etches of high viscosity, and hence extremely thin Te-rich surface films, were found to shunt within a few hours of processing, due to the inability of the thin Te to getter Cu. Devices processed using NP etches of different times, and contacted with Cu-containing graphite paste, initially all showed similar performance. Following stressing, no decrease of V_{OC} or J_{SC} was observed, however, the R_{OC} of devices that had received shorter NP etches had significantly increased, while longer etched samples showed very little change in R_{OC}. These changes are indicative of back contact degradation and again suggest that devices with back contacts processed with thicker Te components will exhibit improved stability due to improved Cu gettering and compensation of other chemical changes.

The chemistry of Cu with Te-rich CdTe surfaces, prepared by different etch treatments, was investigated. The Cu was supplied from graphite paste contacts. Differences in the copper telluride product were observed, dependent on etch type and chemical nature of Cu. The thicker Te-rich layer formed by NP etching results in a higher degree of the CuTe phase, on reaction with Cu-powder or Cu salts in the graphite paste, compared to BM etching. CuCl and CuI appear to form $Cu_{2-x}Te$ on BM etched CdTe, while Cu powder forms CuTe. Initial results were complicated by the presence of residual crystalline graphite from the paste, however this residue can be easily removed.

Effects of stressing cell components and completed devices in conditions of varying humidity were monitored. TeO_2 and $CdTeO_3$ were found to be formed at lower humidities on CdTe, while the formation of amorphous hydroxide, oxide or hydrate phases are more likely at higher humidities. The IEC back contact appears to be stable at higher humidities, but is oxidized to TeO_2 at low humidity. This suggests that copper tellurides are more susceptible to oxidation by atmospheric oxygen. However, despite the extensive chemical changes observed, device performance was almost unaffected. In contrast, First Solar devices showed significant degradation. The robustness of the IEC back contacts is proposed to be due to the thick, 100 nm, Te film present in the back contact, which compensates chemical changes to the contact.

High efficiency CdTe/CdS devices require a robust and durable thin CdS film, which maintains a continuous layer for uniform junction formation. We investigated the relationship between device processing, materials properties and device performance for cells with CdS films deposited by chemical surface deposition (CSD), which produces conformal ultra-thin CdS films with low particulate density and high utilization of Cd

species. In CSD, a solution at ambient temperature is applied to a pre-heated glass/TCO substrate. Film deposition proceeds by heterogeneous nucleation at the surface as heat is transferred to the solution. Heat loss from the solution to the ambient helps maintain conditions favorable for film growth over the time needed typically ~ 5 min. The focus has been on establishing and understanding baseline processing procedures for the CdS/TCO superstrates and post-deposition procedures for completed CdTe/CdS structures. The processing variables investigated here for CdS/TCO were time and temperature of the $CdCl_2$ treatment given to the CSD CdS prior to CdTe deposition and use of a high temperature anneal (HTA) step. Measurements of a film 90 nm thick CdS films on Ga_2O_3/SnO_2/glass before and after vapor $CdCl_2$ treatment at 430°C shows significant recrystallization based on sharpening of the transmission band-edge and sharpening of diffraction peaks (GIXRD). It was found that CdS films grown on Ga_2O_3 have larger grain size than those on glass.

Having established that $CdCl_2$ treatments change the CdS properties, we optimized the device performance by varying $CdCl_2$ temperatures (350-430°C) and times (5-20 minutes). In general, efficiency improved with increasing the temperature and time. Therefore, a temperature of 430°C and time of 20 min was selected for CdS treatment in subsequent studies.

Since the CdS is deposited from a Cl based-solution, it was possible that a HTA would be sufficient to activate the CdS grain growth against further interdiffusion, thus, eliminating the need for a separate $CdCl_2$ treatment of the CdS. Devices were made with and without the HTA and $CdCl_2$ treatments to CdS prior to CdTe deposition. The CdS $CdCl_2$ treatment was at 430°C for 20 min and the HTA was at 550° for 30 min in Ar. Also included in this study were substrates of glass/SnO_2/CdS from First Solar. They did not receive any treatments since the CdS was deposited at high temperature. J-V results showed that cells with the CdS HTA alone or in combination with $CdCl_2$ had reduced FF. The best cell on three identically processed pieces with $CdCl_2$ only (no CdS HTA) ranged from 10-11%. Yields were better than 75%. Cells with HTA had 9-10% efficiency. Devices on First Solar CdS had similar V_{OC} and FF to cells on CSD CdS. We conclude that our CSD CdS is not a major limitation to higher V_{OC} or yield at this time providing it has a $CdCl_2$ pre-treatment.

We are continuing to investigate the relationship between CdTe deposition and film properties for cells with CdTe deposited at a high rate on moving substrates by vapor transport (VT). The VT deposition process is similar but not identical to that used at First Solar. The influence of He and O_2 flow rate (2% O_2/He) and pressure during the CdTe growth was investigated using AFM, GIXRD and contact wetting angle. As compared to the baseline run, increasing the total flow of helium through the source, results in a substantial decrease in grain size. Decreasing the total flow of He yields slightly larger, more densely packed CdTe grains. Increasing the ratio of helium to oxygen by two, results in larger less densely packed grains. Device results from these runs are pending.

The relation between device processing and device performance for cells with VT CdTe deposited at a high rate on moving substrates has focused on establishing and

understanding baseline processing for the post-deposition procedures of completed CdTe/CdS structures. For the CdTe/CdS post-deposition treatments, the time and temperature of the $CdCl_2$ treatment, use of a HTA prior to $CdCl_2$ treatment, and spacing between the $CdCl_2$ plate and CdTe surface were investigated. Following deposition of a ~4 µm CdTe layer at 550°C in a single 6 minute pass in He/O_2 at 20 T, pieces receive a HTA and/or $CdCl_2$ treatment. Contact processing consists of a BDH etch then loading the samples into the evaporator for the layered back contact structure of 50 nm Te, 30 nm Cu, 50 nm Au. Post-contacting annealing was investigated, and a 30 minute anneal in Ar at 190°C was found to be optimum.

The time and ambient of the $CdCl_2$ treatment at 430°C of the completed CdS/CdTe structure was varied from 0 to 60 minutes in either dry or moist air. It was found that the HTA by itself (no $CdCl_2$ treatment) accomplished the same enhancement in performance, to ~8% efficiency, as the optimum $CdCl_2$ treatment in this experiment. A device with neither HTA nor $CdCl_2$ had poor FF and poor collection from the CdTe. There was no clear difference in device performance between dry or moist air during the $CdCl_2$ treatment, suggesting the BDH treatment rendered the CdTe surfaces equally clean in both cases. However, before BDH there were differences in the type of oxides detected by GIXRD and in the surface energy determined by the contact-wetting angle.

It has been shown that O_2 is critical for the $CdCl_2$ treatment to achieve full impact on the device. This leads to concerns about sufficient circulation and replenishment of the O_2 ambient during the $CdCl_2$ treatment in a static system. Humidity and exposure to high temperatures in presence of air can lead to oxide formation on the $CdCl_2$ source plate, leading to concern about their reuse. To study these variables, the spacing between the $CdCl_2$ plate and the substrate was varied during the $CdCl_2$ treatment. Increasing the distance would increase the availability of O_2 at the CdTe surface. Cells made with fresh plates included those with 0 and 6X spacing where X is our standard spacing of ~0.6 mm. After being used for treating the cells with no spacing, the $CdCl_2$ plate was re-used for treating with 2X spacing. It was found that the largest spacing (6X) was best, demonstrating that the delivery of O_2 and $CdCl_2$ are essential to obtaining good device performance. Devices processed with used $CdCl_2$ plates had much lower efficiency and/or severe retrace instability. Following this result, fresh $CdCl_2$ plates were used for every treatment. The best device from this series was VT85.33-01, having V_{OC}=0.749 V, J_{SC}=22.9 mA/cm^2, FF=65.2%, and eff.=11.2%.

CdTe TFP Team Activity and Collaboration

IEC attended the National Team Meeting held at NREL on October 31 and November 1, 2002. We presented a grand summary of stress degradation effects on CdTe cells using data contained in Team Minutes of meetings from 1996 to present. We also presented on effects of post processing and anneal and $CdCl_2$ treatment on BP Solar films, on photoconductivity in CdS films and also on the effects of ambient on CdTe cells during stress treatments. We continued to support BP Solar through collaborative interactions.

We also attended the National Team meeting held at NREL on July 10 and 11, 2003. Two presentations were given, detailing humidity effects during post-deposition processing and stress. Brian McCandless visited First Solar September 23, 2003. IEC has sustained regular interaction with First Solar in the analysis and development of the back contact process. This has included characterization of surfaces by GIXRD, cross-section analysis by AFM, surface energy measurements, compositional analysis of alternative contact materials, and bias-stress studies.

2.3 Phase 3 Summary: 9/5/03 to 9/4/04

During this contract period substantial progress was made in understanding and controlling the CdTe surface chemistry, in determining the effect of humidity and pre-contact CdTe surface condition on stability, in developing transparent ZnTe:Cu contacts, in establishing reproducible CdTe deposition at high rate on a moving substrate in a vapor transport reactor, in making devices with 12-13% efficiency on commercial SnO_2, and in developing new methods for device analysis.

Little is known regarding the effects atmospheric oxygen and humidity on device performance and chemistry during standard stress conditions. We have carried out a systematic investigation of the effects of stress in the dark and light at 80°C at various humidities on IEC and FS CdTe devices. The formation of TeO_2 is observed at 0% humidity but no TeO_2 phases are observed at higher humidities. $Cu_{2-x}Te$ in the back contact is observed at all humidities. The formation of a new phase, $CuTeO_3$, is observed in the pattern for the 0% humidity stressed device. IEC cells exhibited forward-reverse retrace hysteresis prior to stressing which became worse with stressing. The 0% humidity stressed device showed the best stability despite the significant chemistry occurring in back contact during stressing. No back contact changes were detected by GIXRD for the FS stressed devices. All stressed FS devices exhibit J-V rollover at forward bias and decreased V_{OC}, increasing in severity with higher stress humidity. The J-V data of the dark and illuminated humid stressed devices shows similar trends between the two stress conditions, though more rapid degradation is observed for the devices stressed under illumination. We have attributed the improved stability of the IEC devices to the thicker Te, which acts as a sink for excess Cu.

A common etchant used for CdTe device processing is the nitric acid/phosphoric acid mixture (NP), which produces a 50-100 nm crystalline Te layer on CdTe. Experiments were performed to study the autocatalytic nature of NP etching. When using fresh NP solutions it was observed that the etch rates of CdTe were considerably slower than expected. Subsequent etches in the same solution showed faster etching as evidenced by bubbling time, suggesting that a product of the reaction is itself involved in the reaction. Bubbling times were found to decrease with increasing NO_2^-, with almost immediate bubbling observed with treatment of CdTe in NP containing 0.16M $NaNO_2$. From these results, the use of NO_2^- based etchants for CdTe back contacting appears promising and may benefit for CdTe device processing by allowing shorter immersion times, more efficient and controllable etching, and avoiding the use of concentrated HNO_3.

The University of Toledo group has recently presented results regarding a new chemical treatment for CdTe device processing, where samples are illuminated while immersed in an aniline-based aqueous solution. IEC has collaborated with the University of Toledo to assist in understanding of the solution and surface chemistry that may be involved in the aniline-based process. VASE and GIXRD both confirm the presence of crystalline Te ~50-100 nm on the CdTe surface following successful treatments under illumination. Results were very sensitive to the illumination during the treatment. A successful treatment requires the presence of aniline, Cl^- ions, O_2, consistent illumination and careful control of pH. Devices have been processed using aniline treatments under illumination and completed with Cu-containing back contacts and graphite paste. Initial devices show very promising performance, with V_{OC} of ~800 mV, J_{SC} ~20 mA cm^{-2}, and fill factor ~60% or higher. We conclude that a successful aniline treatment of CdTe results in the formation of a crystalline Te-rich surface layer on the CdTe surface, which will be beneficial for back contact processing.

Development of ZnTe:Cu contacts has been motivated by the high p-type conductivity of the ZnTe, needed for low contact resistance, and as a source of Cu doping the CdTe, needed for high V_{OC}. In addition, ZnTe can serve as a semi-transparent back contact for bifacial JV and QE measurements, to provide new insight on the device physics and back junction properties, and as a transparent contact for the top cell of a polycrystalline tandem. During the present contract period, IEC investigated the galvanic solution growth of ZnTe. Tri-ethylamine (TEA) was investigated as a complexing agent to control the chemical reactivity of the Cu in the solution. Cells with optimum TEA had 10% efficiency and negligible hysteresis. The light JV curve indicates a weakly blocking contact when illuminated from front (through glass) but when illuminated from back (through ZnTe) does not have a blocking contact. This indicates that the back contact is photoconductive. Backwall QE measurements through the transparent ZnTe:Cu/ITO shows the response is largely limited to carriers generated very near the CdS junction. There is no evidence of collection at a back junction, nor is there evidence of much collection throughout the CdTe which implies a low lifetime and low field in the bulk of the CdTe.

Increasing V_{OC} with the thin CdS needed for maintaining high Jsc requires reducing the effect of pinholes or regions of non-uniform CdS. The degree of spatial non-uniformity can be directly measured using a modified scanning probe microscope (SPM). We have refined sample preparation procedures to yield polished cross-sections of working cells and have modified SPM for operation in different electrical configurations. Electric field gradient (EFG) measurements have been made with and without additional illumination and at different junction bias. Measurements made at forward and reverse bias and at different illumination conditions revealed marked changes in gradient and have yet to be fully interpreted.

Several baseline VT devices were fabricated to compare with 60 nm thick Ga_2O_3 and In_2O_3 high resistance transparent (HR) layers. CdS films were deposited by chemical surface deposition to a thickness of 100 nm. Cells with a Ga_2O_3 HR layer had V_{oc} of ~0.79 V and efficiency of ~12% while those with an In_2O_3 HR layer had V_{OC} ~0.60 V

and efficiency of 8%. Therefore, Ga_2O_3 HR layers were used in subsequent VT device studies.

Significant design modifications were made to the vapor transport source to increase CdTe utilization and to improve repeatability and overall robustness. The pre-deposition and post-deposition zone heaters were replaced. The new heaters use Tantalum wire looped between a sheet of Vycor glass and a grooved boron nitride plate. A new source was designed and fabricated. The most significant change was the method of delivering heat to the ampoule. Problems with the original design resulted in contamination of the CdTe from the filament as well as significant CdTe deposition onto the inside surfaces of the manifold. The CdTe utilization at the substrate with this source had been 10-20%. The contamination resulting from filament degradation, especially Si and Al, caused shunting and poor efficiency and was verified by SIMS. The new design utilizes a double-wall cylindrical boron nitride source heater to heat the quartz ampoule containing the CdTe charge. Over the range of experimental conditions, re-sublimation of the deposited film is not a critical issue and the CdTe utilization is found to be 50% ± 5%. All films exhibit faceted morphology, with means lateral grain size proportional to film thickness. Grains with lateral dimension comparable to film thickness, ~ 6 μm, are found at 550 and 570°C substrate temperature, but the average grain size is higher and the distribution of sizes is narrower at 570°C.

Alternative processes for treatment in Cl_2 or HCl vapor have also been examined. Two atmospheric pressure approaches for delivery of $CdCl_2$ vapor species were considered: diffusion in parallel-plate configuration and vapor transport via carrier gas in a packed bed. In both approaches, the diffusion of $CdCl_2$ through ambient gas is a critical aspect for estimating concentration at the film surface. Although comparable standard deviations were found for the wet and parallel plate vapor treatments, the highest performance, with efficiency = 12%, V_{OC} > 800 mV and FF > 73%, was obtained with parallel-plate $CdCl_2$ vapor treatment. The cells made with packed bed $CdCl_2$ treatment had lower performance and uniformity.

The sensitivity of cell performance to VT deposition and post-deposition processing, in particular the effect of CdTe growth rate and $CdCl_2$ vapor treatment, was evaluated using CdTe from the newly modified VT reactor. All samples were fabricated on TEC15 soda-lime glass/SnO_2, with 60 nm Ga_2O_3 HR layer and 80-90 nm CdS. The CdTe films were deposited at 20 Torr using He carrier gas and an O_2 base pressure of ~ 0.02 Torr. There are four key conclusions. First, equivalent results were obtained with and without a post-deposition anneal at T>550°C in argon, showing that the anneal step is unnecessary, unlike PVD and electrodeposited cells, in which best results are obtained with an annealing step prior to $CdCl_2$ treatment. Second, cells with no $CdCl_2$ treatment exhibit marked photo-response, indicating that the high deposition temperature yields an active junction, again in contrast to PVD or electrodeposition. Third, similar results were obtained over the range of static equivalent growth rate, from 7 to 12 μm/min and deposition temperature, from 550ºC to 570ºC. Fourth, nominally similar performance was obtained for vapor $CdCl_2$ treatment from 405ºC to 425ºC for 20-25 min but the highest V_{OC}'s were obtained over a narrower range, from 405ºC to 410ºC. Cells with no

post-deposition Cl treatment exhibited the lowest blue response (thickest CdS) and the lowest absorber band edge (highest band gap), consistent with no CdS diffusion into the CdTe. The other samples show a similar range of blue response and similar long wavelength fall-off, consistent with CdS loss ≈ 10 nm and formation of $CdTe_{1-x}S_x$ with x < 0.05, respectively. QE measurements at reverse bias confirm that losses in J_{SC} are due to absorption not collection losses. Devices with V_{OC}>0.80 V and FF>68% were obtained on pieces from multiple runs using Au/Cu evaporated contacts. The highest efficiency was on piece VT118.4 with Voc=0.808V, Jsc=23.8 mA/cm2, FF=69.2%, and efficiency=13.3%.

Voltage dependent photocurrent collection losses can be especially significant in CdTe solar cells, primarily reducing the fill factor. We analyzed the $J_L(V)$ effect in CdTe solar cells by measuring current-voltage curves J(V) at different intensities and using the difference to quantify $J_L(V)$ similar to previous work at IEC on CIGS. We have analyzed over 10 CdTe devices from 4 different CdTe sources having FF from 50 to 72 and thicknesses from 1.8 to 5 µm. All show significant $J_L(V)$ losses affecting the maximum output power and FF. Recalculating the FF without these losses results in a 5-15% point increase. Voltage dependent collection in CdTe solar cells increases after stressing. This effect is well described using the uniform field model as was developed for *p-i-n* solar cells. Numerical simulations with AMPS support the experimental results.

Measurements of V_{OC} (T) shows linear fit from 220 to 320K on most CdTe devices over a range of intensity with an extrapolated intercept of ~1.5 eV consistent with the CdTe bandgap. However, we have found that at lower temperatures, the V_{OC} becomes independent of light intensity and temperature, saturating at about V_{OC}=1.0 V. We suggest that this upper limit represents a fundamental parameter, the built-in voltage. Saturation of V_{OC} indicates carrier freeze-out. When there are no longer sufficient free carriers, the quasi-Fermi levels no longer respond to changes in carrier generation or temperature. V_{OC} reaches its maximum value determined by the absorber bandgap and the contact potentials. The saturated value of V_{OC} decreases after stress from ~1.0V to ~0.90-0.95 V.

CdTe TFP Team Activity and Collaboration

The Institute has maintained a high level of collaboration with CdTe Thin Film Partnership team members. Towards the goal of helping First Solar to develop vapor $CdCl_2$ treatments, IEC: constructed a new $CdCl_2$ source generator at IEC to carry out experiments compatible with First Solar; carried out experiments to directly compare treatment in $CdCl_2$ vapor with treatment of $CdCl_2$-coated samples; submitted detailed reports on modeling $CdCl_2$ vapor delivery; and investigated source-poisoning issues associated with oxide formation in the source generator. IEC performed GIXRD measurements on a large number of CdTe films at different stages of processing and for different back contact processing conditions. IEC characterized the structure and composition of the back contact surface of First Solar production plates and of newly developed contacts made by a third party company for First Solar. IEC has also been

assisting in the analysis of CdS film properties, CdTe-CdS interaction after processing, and CdS/TCO quality assurance issues for First Solar. IEC received a set of samples from First Solar including baseline devices, as well as those having unusual J-V performance. Complete analysis of J-V-T and QE(V) was performed and reported at the team meeting along with results on similar samples by CSU and USF.

Collaboration with Canrom has also been on-going, with respect to post-deposition processing methods for Canrom CdTe/CdS and to the Team-related issue of evaluation of humidity during cell stress. This follow-up to the samples stressed in the dark at 85°C at different humidities consist of repeating the stress conditions but in the light with the calls at V_{OC}. Results were presented at the team meeting and in this report.

We also provided devices to CSM for cross-sectional luminescence measurements.

Four members of IEC (Darshini Desai, Kevin Dobson, Brian McCandless and Steve Hegedus) attended the CdTe National Team Meeting in Toledo, February 2004. Much of the work presented there is also contained in this report. Topics included the chemistry of the aniline bath treatment of CdTe, the effects of humidity stress of CdTe under illumination; temperature dependence of Voc to characterize recombination; voltage dependence of photocurrent to evaluate FF losses; and work related to the FS vapor-$CdCl_2$ treatment.

2.4 Phase 4 Summary: 9/5/04 to 9/4/05

Research on CdTe-based solar cells includes five tasks: (1) High Throughput CdTe Processing; (2) Back Contact Processing Options; (3) ZnTe:Cu Semi-Transparent Contacts for Bifacial Device Analysis; (4)Understanding and Improving V_{oc}; and (5) Accelerated Stressing.

Processing options, which address a number of critical issues relating to processing of thin-film CdTe/CdS devices have been addressed. The window layer properties, including configuration, composition and thickness have been shown to have a significant effect on final device performance. We have selected Ga_2O_3 as the best high resistance interface layer for our process. Engineering and thermo-chemical aspects of the post-deposition $CdCl_2$ treatment of CdTe were investigated. Annealing CdTe films in the presence of $CdCl_2$ and O_2 promotes CdS diffusion into CdTe and also shifts the chemical equilibrium of the film surface, which may influence the bulk electrical properties of the CdTe. Comparisons of wet and vapor $CdCl_2$ treatment were discussed including the development of a packed bed reactor for vapor $CdCl_2$ treatments. High efficiency with good spatial uniformity was achieved with vapor $CdCl_2$ treatment. Careful control of the O_2 and humidity in the anneal atmosphere is required to avoid the formation of deleterious oxides, which will affect the Cd-vacancy concentration within the CdTe film, leading to poor device performance. High throughput was evaluated by increasing the CdTe deposition rate to 9 µm/min, reducing the $CdCl_2$ treatment time while increasing the treatment temperature, and reducing the CdTe thickness. VT devices with 5-7 µm

thick CdTe deposited on moving substrates at 9 μm/min using a 20 min vapor $CdCl_2$ treatment at 415ºC achieved V_{oc} up to 840 mV and efficiency > 13%. Devices with efficiency of 11% were obtained with 2 min $CdCl_2$ treatments at 465ºC. For cells with CdTe thickness ~1.5 μm, efficiency >10% was obtained . V_{oc} and FF decreased for cells with CdTe deposited at >80 μm/min and for cells with CdTe thinner than 1.5 μm.

A number of steps are required for successful processing of back contacts to CdTe; removal of any oxides, the formation of a Te-rich surface, application of a Cu source, contact annealing and deposition of a secondary contact. A number of methods can be used for each of these steps. Consideration of different processes should include simplicity and ease of industrial scale up. The nature of each process may also be critical for contact and device stability. A thorough knowledge of etching mechanics will allow the development of alternate or modified etches that may be more efficient and faster, perhaps through the use of catalysts, and safer to use, all of which will assist possible industrial scale-up of CdTe technology. The results obtained from monitoring the etching processes have also highlighted the usefulness of VASE and GIXRD as diagnostic tools for monitoring the quality of material surfaces during processing.

The Te rich surface can be formed by wet chemical etching or by 'dry' deposition of Te, however, application of Cu should be carried out immediately, to prevent atmospheric oxidation of the Te-rich surface. A number of simple methods of Cu application have been studied including Cu metal, CuCl doped graphite, dipping in CuCl, and Cu-doped ZnTe. Contact annealing should be carried out in an inert atmosphere to avoid oxidizing the back contact. A full understanding of the role of Cu and other possible contact metals in the back contact chemistry and their behavior within the CdTe/CdS structure is required before optimization of device performance and stability can be obtained.

The use of an aniline-based treatment for back contact processing of CdTe/CdS devices was investigated. The treatment was found to form reproducible Te-rich CdTe surfaces, similar to oxidizing etches, which would be expected to allow processing of improved Cu-based back contacts. Analysis of bath conditions highlights that the presence of aniline, Cl^- ions, dissolved O_2, consistent illumination and control of pH are critical for successful treatments. A photocatalytic mechanism is proposed, involving the reduction of dissolved O_2 by conduction band electrons to produce H_2O_2 or similar, which etches the CdTe. The reduction is complemented by the oxidation of aniline by valance band holes. Best device results, with efficiencies ~12%, have been obtained for treatment times as short as 30 min. At longer treatment times, device performance decreases, though the effect is not as severe as has been observed with over-treatment of CdTe in oxidizing etches. Criteria for possible substitutes for the toxic aniline are presented. Results of potential substitutes are discussed. A crucial advantage of aniline is that it is compatible with thinner CdTe films. Unlike more aggressive etches like BDH or NP, aniline etching gives a high yield and negligible shunting with CdTe devices < 3 μm thick.

Cu-doped ZnTe films grown by galvanic deposition were developed to provide transparent ohmic contacts to CdTe solar cells. Control of the Cu doping with

triethanolamine was critical to limit the free Cu in order to achieve high transparency (>60% in the visible) and to minimize shunting. Devices with ZnTe:Cu contacts had comparable performance to devices with Cu/Au or Cu/Ni contacts, achieving V_{OC} of 0.82 V and fill factor (FF) of 68% for standard front illumination. The ability to form a low barrier, Ohmic contact with ZnTe:Cu depends on the CdTe surface treatment and results in formation of a thin Cu_2Te interlayer, verified by GIXRD. Typically, devices with BDH or anilene treatments had better forward bias behavior and do not exhibit roll-over beyond V_{OC}, indicating an ohmic low barrier contact has been formed. Devices with Br-methanol had lower FF and exhibited rollover. Bifacial spectral response (SR) measurements, through front and back contacts, were analyzed and yielded a diffusion length (L) of 0.8 µm and depletion width (W) of 2.5 µm for 5 µm thick CdTe cells. Backwall SR measurements made through the transparent ZnTe contact are much more sensitive to L and W than are measurements for standard front illumination. ZnTe:Cu is a promising material for bifacial characterization as well as tandem cell interconnects and more stable Cu-doped contacts. Characterization of devices with CdTe layer thickness from 1.5 to 10 µm is in progress. Accelerated stress testing on devices with ZnTe:Cu contacts with different concentrations of Cu is planned.

Changing the bias voltage, light intensity and temperature during stress can induce transient degradation or recovery in V_{OC} of CdTe solar cells. Simulated day/night cycles leads to daily degradation in the light and recovery in the dark. Greater recovery in the dark and less bias dependence is correlated with better overall stability. These transients complicate the correlation between cell (indoor) and module (outdoor) performance. Results are consistent with changes in electronic states and recombination. No single stress protocol is likely to identify all instability mechanisms.

Increasing V_{OC} in VT CdTe/CdS cells to >900 mV and maintaining it in cells with sub-micron thick CdTe layers requires an understanding of existing cells, determination of the recombination sources in the cell, quantifying the influence of back contact on V_{oc}, especially in thin devices, and assessing changes induced by depositing onto a moving substrate at elevated rate (>10 µm/min). The problem has two parts: 1) defining limits to V_{oc} in CdTe solar cells in general and 2) defining the influence of VT processing, especially in thinner cells.

We have found that the following empirical factors affect V_{oc} in present-generation VT CdTe devices. When initial $d_{CdS} < 80$ nm or final $d_{CdS} < 40$ nm, a buffer layer is needed to maintain V_{oc}. The highest V_{oc} is obtained for CdTe deposition >500ºC. V_{oc} decreases as CdTe thickness decreases to $d_{CdTe} < 1.5$ µm. Thinner CdTe requires re-optimization of the $CdCl_2$ temperature time cycle and a less penetrating surface etch, such as anilene instead of BDH. The $CdCl_2$ surface is critical to device performance with aging reducing the effectiveness of the $CdCl_2$ treatment, including reduction in V_{oc} and yield. High V_{oc} requires an O_2 partial pressure during VT growth. Cu in the contact does not appear to be necessary for $V_{oc} \sim 0.78$V but Cu + HT is necessary for $V_{oc}>0.80$V. We have determined that a back contact barrier has no effect on V_{oc}, at least for devices with 3-4 µm CdTe, consistent with recontacting studies from several years ago. Eliminating voltage dependent collection has little effect on improving V_{oc} on devices with FF>65% but can

have significant improvement on cells with FF<60%. The upper limit to V_{oc} obtained at low temperature is around 1 V, suggesting this is the built-in potential. The highest V_{oc} at 28°C obtained this year was 0.84V.

CdTe TFP Team Activity and Collaboration

Support of the National CdTe R&D team continued through sub-team leadership, bifacial and stress analyses, and film/cell supply to other team members. Unprocessed and $CdCl_2$ treated PVD and VT CdTe/CdS stacks were sent to Colorado State University for photoluminescence investigations of defects. Completed devices were sent to Colorado School of Mines for investigation of defect levels by admittance spectroscopy. The cell fabrication matrix evaluated was: with/without $CdCl_2$ treatment, with/without Cu, and with less and more intrusive etching prior to metallization. Preliminary results of these studies were presented at the Team meeting held in May 5-6, 2005. IEC made presentations at the team meeting: "Bifacial CdS/CdTe/ZnTe Device Characterization", "Effect of Applied Bias during Stress", and "Sensitivity of CdTe/CdS Device Operation to Processing Variations". IEC provided extensive analysis of Cu_xTe back contacts developed by Ceramem Corporation using nanoparticle precursors. On-going collaboration with the University of Toledo continued on the fundamental surface chemistry associated with aniline treatments. IEC also conducted bias-dependent tensile pull tests of as-deposited and stressed UT cells to elucidate changes induced by processing and stress variations. In these cells, the adhesion of all layers was sufficiently high that failure occurred either at the epoxy-cell interface or via glass cracking, which is a tacit demonstration that cells with metallized contacts can exhibit high mechanical durability. Other activities included providing VT samples to McMaster Energy Enterprises (aka Solar Fields) for start-up development of post deposition processing, providing NREL with technical details of the IEC VT system, and teaching the chemical surface deposition (CSD) technique to several groups.

2.5 Phase 5 Summary: 9/5/05 to 3/31/07

The CdTe cell fabrication effort focused on CdTe deposition and post deposition processing to increase throughput by decreasing processing step time and reducing CdTe film thickness. Effort was also directed at handling and processing issues which affect baseline cell efficiency. The effect of carrier gas composition and substrate temperature on vapor transport (VT) CdTe film growth and device performance was evaluated. Vapor $CdCl_2$ treatments, which allow the treatment temperature to be separated from the $CdCl_2$ and O_2 concentration, were refined to allow a new baseline process to be defined with treatments ~ 2 minute in duration. Reduction in treatment time required increasing the treatment temperature of the CdTe/CdS and maintaining the partial pressures of $CdCl_2$ and O_2 to ~5 mTorr and 120 Torr, respectively. Similarly, the aniline photo-activated surface treatment was refined to permit effective Te formation in less than 5 minutes, by increasing the intensity of the incident light. In the area of device performance, analysis of J(V) curves has indicated that most CdTe cells can be described with three circuit elements: by a single forward diode (given by A, J_o), a resistance (R),

and a voltage dependent photocurrent ($J_{L0} * \eta(V)$). Systematically determining these parameters and evaluating their impact on efficiency shows that our typical VT device with 13% efficiency could be 16% efficient in the absence of R and voltage dependent collection. This sets an upper limit based on the junction recombination.

Different aspects of processing VT solar cells were evaluated, and new processing options to address key issues of high throughput are being developed. In particular, variations in device performance are correlated with systematic variations in the $CdCl_2$ treatment and with the exposure of fresh CdTe surfaces to humid ambient prior to $CdCl_2$ treatment. With respect to CdTe deposition, characterization of the VT deposition system was carried out to refine the quantitative model used to monitor the deposition rate and Cd utilization. With respect to surface treatments for back contact processing; alternatives to BDH processing, such as aniline treatment, continue to be investigated. Temperature dependant bifacial QE measurements gave new insights into the CdTe device physics. The formation rate and composition of oxide phases in CdTe films was further quantified with respect to humidity.

Voltage dependence of the photocurrent $J_L(V)$ of CdTe/CdS solar cells has been characterized by separating the forward current from the photocurrent at several intensities. The primary mechanism of photocurrent collection in CdTe solar cells illuminated through the front CdS is field-assisted drift in the depletion region. $J_L(V)$ reduces the fill factor (FF) of typical cells by 10-15 points, the open circuit voltage (V_{OC}) by 20-50 mV, and the efficiency by 2-4 points. A single carrier Hecht model developed for drift collection in *p-i-n* solar cells gives a good fit to the data for CdTe thickness from 1.8 to 7.0 μm and yields a fitting parameter consistent with lifetimes of 10^{-9} sec, as measured by others. Accelerated thermal and bias stressing increases $J_L(V)$ losses.

Bifacial analysis provides quantitative insight into CdTe device operation by separating the effects of front and back junction. Semi-transparent ZnTe:Cu contacts were developed and applied to CdTe devices with varying thickness (t) to determine the diffusion length (L), and depletion width (W) from analysis of the back spectral response (SR_B). Front spectral response (SR_F) is nearly unaffected by L. SR_B and back J_{SC} are higher for thinner cells as SR_B is limited by diffusion across the field free region that is smaller for thinner cells. Bifacial characterization results indicate a photosensitive back barrier. There is no evidence of a back junction in these cells. A single junction determines recombination current.

CdTe TFP Team Activities and Collaborations

Collaborations under the Thin Film Partnership were conducted with groups at the University of Toledo (UT), Colorado School of Mines (CSM) and at the National Renewable Energy Laboratory (NREL). CdS films on Ga_2O_3-coated TEC15 and Ga_2O_3/ITO-coated flexible Pilkington glass substrates were sent to UT for stress-piezoelectric analysis and device fabrication. Completed VT cells fabricated with and without $CdCl_2$ treatment and Cu contacts were supplied to CSM for admittance

spectroscopy analysis in an effort to correlate these processing variables with the spectral signatures indicative of defect levels. Several sets of VT devices were fabrication using TCO and TCO/HR and TCO/CdS provided by the CdTe group at NREL. IEC attended the National CdTe R&D Team meeting on March 9-10, 2006. Brian McCandless co-led the Materials Chemistry sub-team with Tim Ohno (CSM) and made presentations in sessions for the Device Physics and Materials Chemistry teams and at a workshop focused on CdTe solar cell open circuit voltage.

2.6 Phase 6 Summary: 4/1/07 to 12/31/07

The CdTe task focused on aspects of cell fabrication that can be used to improve module performance and utilize thin CdTe absorber layers, to increase processing throughput and reduce materials usage. Issues related to high throughput processing of and junction-limiting factors in CdTe solar cells are reported. Based on the effects of TCO/substrate cleaning described in the previous annual report, we continued with the study of uncontrolled impurities originating in the glass/SnO_2 substrate. Concerns over possible sources of impurity contamination of CdTe has prompted further analysis of the influence of soda lime glass (SLG) SLG/SnO_2 substrate preparation as well as the chemistry of the CdS growth and its effect on the CdS-CdTe junction region. It is vital that this source of variability in film morphology and device performance is eliminated prior to development of cells with sub-micron absorber thickness and evaluation of approaches for V_{OC} > 900 mV. In this report we present the details of procedures used to establish a performance baseline with cell efficiency >11% for processing CdTe/CdS cells with vapor transport deposited CdTe onto moving substrates at high growth rate (~10 μm/min) using rapid post-deposition processing, with less than 1 min per processing step. CdTe films having low pinhole density, $<10^{-6}$ fractional area, are routinely deposited by vapor transport over a thickness range from 1 to 10 microns. Issues related to high throughput and high temperature processing of and junction-limiting factors in vapor transport deposited thin film CdTe solar cells are reported. CdTe/CdS cells deposited onto commercial soda lime glass substrates films by vapor transport deposition and processed with 1 min $CdCl_2$ treatments with 3 micron and 1 micron thick CdTe have achieved AM1.5 conversion efficiencies of >11% and 7%, respectively.

CdTe TFP Team Activity and Collaboration

IEC continued interaction and collaboration with (former) CdTe R+D Team members. Specifically, we provided guidance to Primestar Solar for materials and equipment needed to develop CdTe deposition and post-deposition processing. We continued collaboration with Alan Fahrenbruch regarding analysis of back contact barriers to CdTe and the sensitivity to composition for Cu-Te contacts.

2.7 Phase 7 Summary: 1/1/08 to 5/31/08

Thin CdTe Absorbers

CdTe films were deposited by vapor transport (VT) from a single compound source. This method provides several key control parameters for adjusting growth rate and thickness: 1) translation speed; 2) source temperature; 3) carrier gas flow rate; 4) total system pressure; and 5) substrate temperature. For this work, translation speed was fixed at 2 min per plate, and source temperature was used to adjust the incident flux at the substrate. The total system pressure was 20 Torr, substrate temperature was 550°C, carrier gas flow rate was 20 sccm. CdTe source temperature was varied from 830°C to 800°C to control deposition rate. Thermal loading on the inlet side of the source cools the source by ~20°C, resulting in a thickness gradient perpendicular to the translation direction along a 2 cm wide band of the otherwise uniform substrate. Thus a single 10 x 10 cm plate carries a CdTe film with uniform thickness over a 10 x 8 cm portion, and a narrow band of graded thickness.

VT CdTe films were deposited onto 10 x 10 cm commercial soda-lime glass (SLG) substrates translating beneath the CdTe source as described previously.[1] The superstrate devices consist of SLG/SnO_2/HRT/CdS/CdTe with Cu/C contacts, where the CdTe received post-deposition treatment at 1 atm in Ar/O_2 containing $CdCl_2$ vapor generated from a sublimation source.[2] The SLG/SnO_2/HRT substrates are Pilkington TEC15, coated with either high resistance Ga_2O_3 or ITO. The 90 nm thick CdS films were deposited by chemical surface deposition and received vapor $CdCl_2$ treatment at 400°C prior to CdTe deposition. Baseline CdTe films ~5 μm thick are routinely deposited using a source temperature of 830°C at a growth rate of 10 μm/min. Thinner films, as thin as 0.3 μm, were obtained by reducing the source temperature to 790°C.

CdTe films were examined for pinholes with lateral size from 1 to 50 μm using white light transmission. Pinhole counts exceeding 5 per plate were only found on depositions run immediately after source ampoule changes, due to dislodged particulates, and such plates were rejected for processing into completed devices. Otherwise, plates exhibited only 1-5 pinholes in the CdTe film over the entire surface, independent of thickness. CdTe film morphology was analyzed by atomic force microscopy (AFM) in tapping mode using a Digital Instruments Nanoscope IIIa Dimension 3100. The grain size distribution was determined from AFM scans covering a 20 x 20 micron region (Figure 1) on each sample by binning grains into size categories. The grain size distributions of thin CdTe films, with thickness from 0.3 μm to 3 μm, are shown in Figure 2 and approximate log-Normal distribution with peaks indicative of height/width ratio ~2X. Films with 0.3 μm to 0.5 μm thickness exhibit nearly-identical frequency distributions and conform to the underlying SnO_2. The r.m.s. roughness on bare SnO_2 and on the CdTe films with thickness from 0.3 μm to 0.8 μm was 35 nm ± 5 nm. CdTe surface roughness increased proportionally with thickness for films from 1 μm (r.m.s. = 50 nm) to 5 μm (r.m.s. = 90 nm).

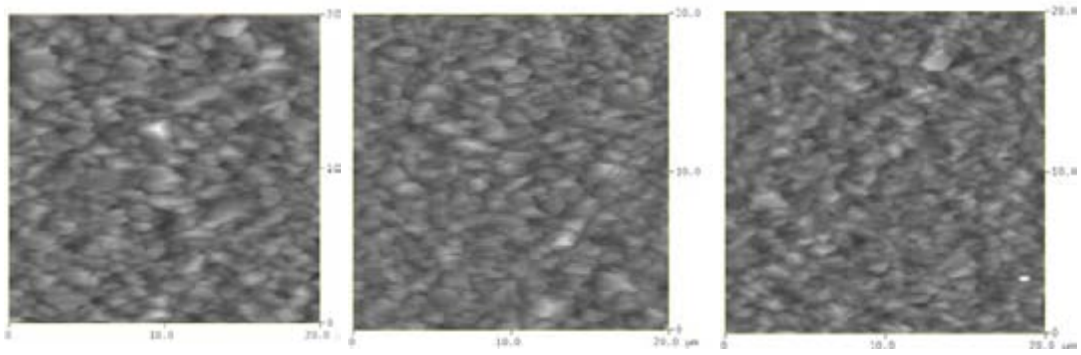

Figure 1. Tapping AFM images of CdTe surface (20 x 20 μm) for thin CdTe films: 1 μm (left), 0.8 μm (center) and 0.5 μm (right) VT films deposited at source T_{sou} = 800°C and substrate T_{sub} = 550°C.

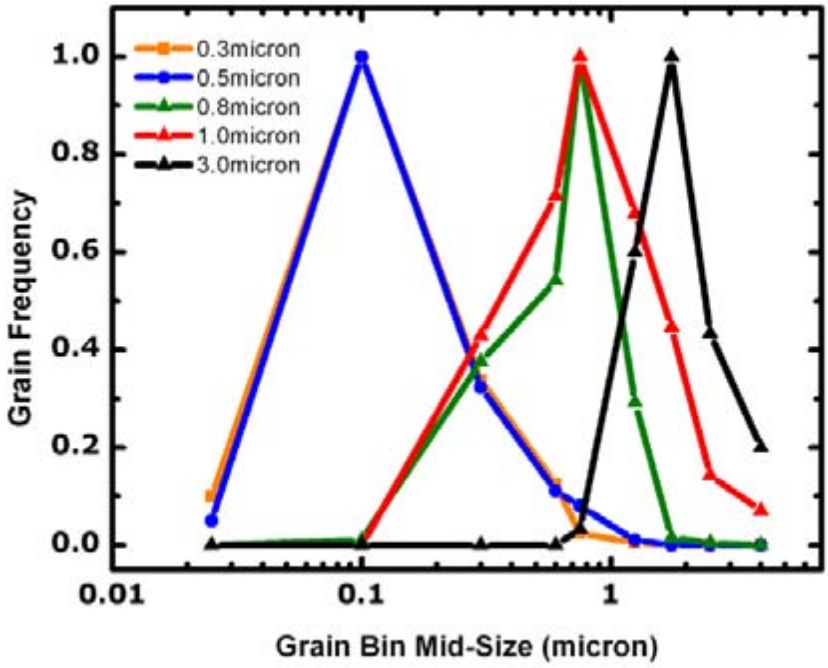

Figure 2. Grain size distribution of VT CdTe films with thickness ranging from 3 to 0.3 μm.

Optical transmission (T) and reflection (R) were measured using a Perkin-Elmer Lambda-9 spectrophotometer from 400 nm to 1000 nm. T/(1-R) is shown in Figure 3 for SLG/SnO_2/ITO/CdS/CdTe structures with CdTe thickness from 0.3 μm to 3 μm. Long wavelength transmission increases with decreasing film thickness. The loss in photocurrent for single-pass absorption is estimated from the transmission data by integrating the transmission with the AM1.5 spectral output. The effect of reducing CdTe on short circuit current (J_{SC}) in cells is listed in Table I for several films of Figure 3. No significant change in photocurrent is expected from baseline thickness down to 1

μm. Photocurrent losses from 1 mA/cm^2 to ~4 mA/cm^2 are expected for films with thickness below 1 μm assuming no change in junction behavior, the maximum V_{OC} change due to the decrease in J_{SC} is ~50mV over the thickness range.

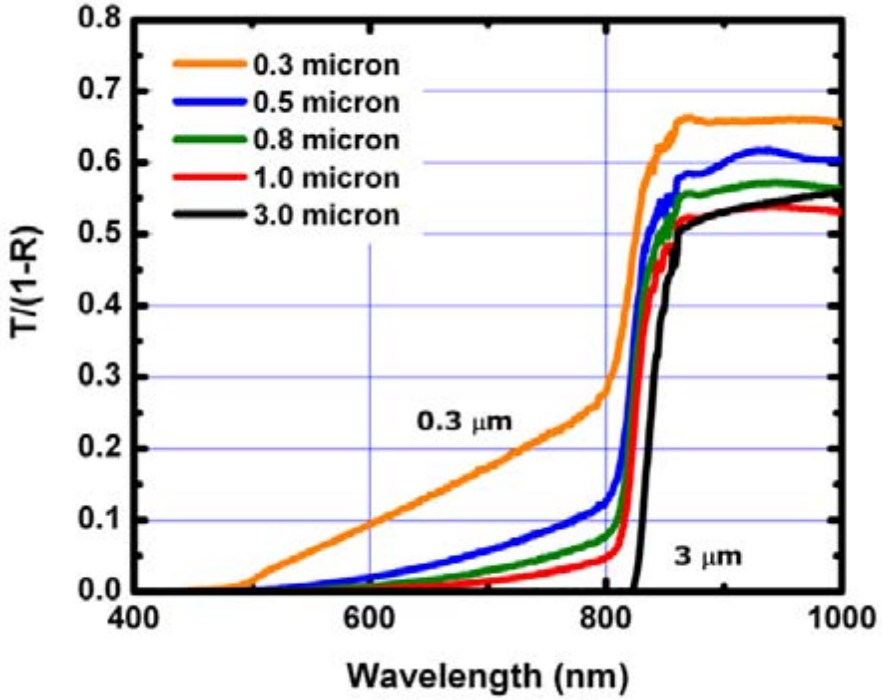

Figure 3. Normalized optical transmission T/(1-R) versus wavelength of SLG/SnO_2/Ga_2O_3/CdS/CdTe structures with CdTe film thickness ranging from 0.3 to 3 μm.

Table I. Calculated AM1.5 J_{SC} loss for data of Figure 3.

CdTe Thickness (μm)	J_{SC} Loss (mA/cm^2)
3.0	0
1.0	0.3
0.8	1.1
0.5	1.8
0.3	3.6

The primary objective of this sub-task is to specify deposition and vapor $CdCl_2$ post-deposition treatment conditions needed for high throughput processing (1-2 min per plate) of polycrystalline thin film CdS/CdTe solar cells with sub-micron CdTe. This requires characterization of the grain size distribution obtained during CdTe film growth which affects the delivery of $CdCl_2$ and O_2 to the CdTe film and influences CdTe-CdS inter diffusion. VT deposition allows great flexibility in CdTe film growth, with static

deposition rates up to ~100 μm/min. However, cells with thin absorbers and deposited at high translation speeds do not require such high growth rates to obtain high throughput, so lower source temperatures can be employed for CdTe film growth.

In polycrystalline CdTe films, the chemical reactivity obtained during treatment is enhanced by the presence of grain boundaries, which allow $CdCl_2$ and O_2 to penetrate the film, reach the CdS-CdTe interface and react along grain surfaces. The fractional grain boundary volume increases as grain size decreases. For a tessellated hexagonal array of uniform grains with 1:1 aspect ratio, a decrease in film thickness produces a decrease in lateral grain size. For a reduction from 10 μm to 0.5 μm, the contact perimeter increases from 60 μm to 140 μm and ratio of grain boundary to grain volume increases from 0.004 to 0.7. The optimization of superstrate CdTe/CdS solar cells is accomplished by a combination of surface reaction and diffusion. The diffusion of defects from CdTe grain surfaces into grain interiors is driven by the concentration gradient on the CdTe surface and along grain walls. The time needed to diffuse defects into grain interiors relies on the diffusivity of cadmium vacancies (V_{Cd}). At the same time, the thermodynamic driving force for CdS-CdTe intermixing drives interface diffusion, limited by Cd self-diffusion through the CdTe lattice. By specifying the processing time, the problem is to find the bulk diffusion coefficient (D_B) needed to accommodate the particular grain size distribution and specified processing time,

$$D_B = \frac{r^2}{\tau} \quad (1)$$

where r is half the grain size and τ is the characteristic time. For the example of films with 10 μm and 0.5 μm grain size, the characteristic diffusion time at constant temperature is reduced by 400X. Although the bulk diffusion coefficients for V_{Cd} are unknown, the optimization process for solar cell performance controls Cd self-diffusion; likely the slowest process and is therefore a reasonable limit. Also, the consumption of CdS needs to be considered as the grain size or temperature is changed. Therefore, processing temperatures follow from the bulk diffusion process for Cd self diffusion and the grain boundary diffusion process for CdS in CdTe (D_{GB}):

$$D_B = 2.4\text{x}10^7 e^{-\left(\frac{2.8}{kT}\right)} \text{ cm}^2/\text{s} \quad (2)$$

$$D_{GB} = 3.4\text{x}10^6 e^{-\left(\frac{2.0}{kT}\right)} \text{ cm}^2/\text{s} \quad (3)$$

for treatment in 9 mTorr $CdCl_2$ and 150 mTorr O_2. D_{GB} depends on $CdCl_2$ partial pressure (P_{sat}) over the range 1 to 100 mTorr:

$$D_{GB} = 9.0\text{x}10^4 P_{sat}^{2.73} e^{-\left(\frac{2.0}{kT}\right)} \text{ cm}^2/\text{s} \quad (4)$$

Only the grain boundary diffusion, via surface reactions is sensitive to both $CdCl_2$ and O_2 concentration. For CdTe films deposited by VT at 550°C processing with vapor $CdCl_2$ treatment in the 1-2 min time frame is considered. The properties of solar cells fabricated with these films are reported and discussed with respect to the absorber thickness.

The vapor treatment method allows $CdCl_2$ concentration to be independently controlled from the CdTe/CdS sample temperature. As found with conventional $CdCl_2$ treatment, the vapor $CdCl_2$ treatment promotes diffusion of CdS into CdTe films. For VT CdTe films deposited at 550-600°C in N_2/O_2 ambient, no grain growth is detected following the $CdCl_2$ treatment, indicating that as-deposited VT CdTe films are in a low energy state compared to PVD films of the same thickness. 3D modeling of CdS diffusion into CdTe using measured grain size distributions shown in the previous report (for January 2008 of this contract) and previously determined bulk and grain boundary diffusion coefficients and activation energies (Equations 2-4 above), the temperature-time conditions were determined to produce similar diffusion profiles but at markedly reduced processing time.

Fig. 4 shows calculated $CdTe_{1-x}S_x$ depth profile plots (c/co versus depth) for films from 5 to 0.5 μm thickness using the measured grain size distributions of VT CdTe films with the corresponding thickness, calculated for baseline vapor $CdCl_2$ treatment under the following conditions: isothermal vapor $CdCl_2$ treatment at 420°C for 20 minutes (420°C/20 min) at 1 atm, with 150 mTorr O_2 partial pressure. In this case, the $CdCl_2$ partial pressure is 9 mTorr and the bulk and grain boundary diffusion coefficients used were: $D_B = 1.2 \times 10^{-13}$ cm^2/s and $D_{GB} = 1.1 \times 10^{-8}$ cm^2/s, respectively. In the figure, the bulk and grain boundary contributions are apparent by the steep and flat regions, respectively. For films <3 μm, thick, the bulk contribution is more apparent due to decreasing lateral dimension compared to the bulk characteristic diffision distance. Integration of the curves with the $CdTe_{1-x}S_x$ solubility limit at 420°C (x = 0.06) allows the equivalent CdS film consumed to be estimated and is indicated on the right side of the plot. For the typical baseline film (5 μm) treated at 420ºC for 20 minutes, the least alloy formation is obtained, with an equivalent CdS film thickness consumed of only 20 nm. This corresponds extremely well to the measured final CdS thickness after cell fabrication and physical removal of the $CdTe_{1-x}S_x$ absorber layer. For the thinner CdTe films, the equivalent CdS thickness consumed is slightly greater and shows that uniform $CdTe_{1-x}S_x$ alloy production is expected for films > 0.5 μm thick.

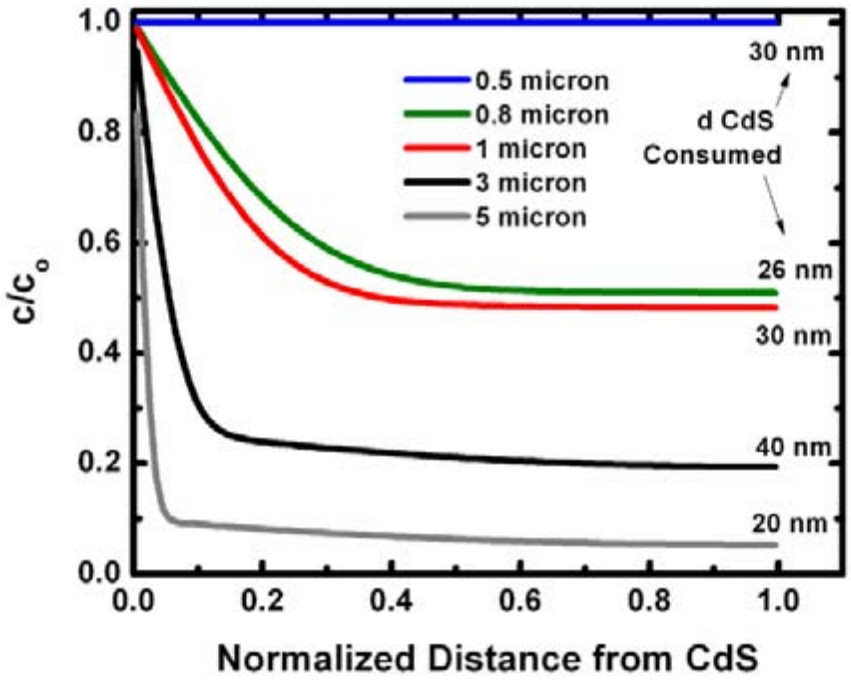

Figure 4. Calculated S concentration (c/co) versus normalized distance from CdS-CdTe interface for CdS/CdTe couples with different CdTe thickness. The calculation used the measured grain size distribution and diffusion coefficients corresponding to baseline vapor $CdCl_2$ treatment at 420°C for 20 minutes.

Reduced vapor $CdCl_2$ treatment time is facilitated by increasing reaction temperature without changing other parameters. For example, with a 5 μm CdTe film; nominally similar CdS consumption is obtained for temperature/time treatments of 420ºC/20 min, 480ºC/2 min, and 495ºC/1 min in 9 mTorr $CdCl_2$ and 150 Torr O_2. For the shorter cases, at 480ºC for 2 minutes and 495ºC for 1 minute, the equivalent CdS thicknesses consumed is 2X higher, ~40 nm. An extreme case, at 480ºC for 20 minutes, shows consumption of 100 nm of CdS, which would eliminate the CdS layer in these 5 μm thick devices. Extending these calculations to thinner films using Equations 2-4 to find D_B and D_{GB} enables benchmark treatment temperatures to be specified for 2 min treatments (Table II).

Table II. Temperature benchmarks for vapor $CdCl_2$ treatment of CdS/CdTe with different CdTe thickness.

CdTe Thk (μm)	T Reaction (°C)	T $CdCl_2$ (°C)
5	480	420
3	475	420
1	470	415
0.8	465	415
0.5	460	410
0.3	460	410

The AM1.5 performance of baseline (5 μm thick CdTe) VT CdTe cells fabricated with vapor $CdCl_2$ treatment at 480ºC with $CdCl_2$ time from 1 to 4 min is shown in Table III. The quantum efficiency (QE) at $\lambda = 400$ nm provides a quantitative measure of the final CdS film thickness. In the table, the final CdS film thickness decreases progressively with increasing treatment time over the treatment time range. Given that the starting CdS thickness was 90 nm, the quantity of CdS consumed is comparable to that predicted by the diffusion model above for 5 μm thick films. The cell performance data shows that optimal V_{OC} is obtained for 2-4 min treatment while optimal FF is obtained for 1-2 min treatment. Although the CdS thickness was slightly affected by the treatment time, the J_{SC} was not significantly different.

Table III. Best-cell J-V results for VT cells with baseline 5 μm CdTe deposited and vapor $CdCl_2$ treatment at 480ºC with different $CdCl_2$ time.

$CdCl_2$ HT (min)	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	η (%)	QE @ 400nm (%)	Final dCdS (nm)
1	783	23.6	66.6	12.3	40	60
2	796	24.3	69.4	13.4	42	58
2	813	23.6	66.2	12.7	44	55
2.5	800	23.3	65.1	12.2	44	55
4	819	24.3	64.6	12.9	50	35

The treatment conditions of Table II were adopted for the fabrication of solar cells with thinner VT CdTe absorber layers. The effect of the BDH etch process was evaluated on samples with different CdTe absorber thickness and 2 min treatment time. A small sample set was sufficient to indicate a dramatic drop in both V_{OC} and FF for cells with absorber thickness <2 μm (Fig 5). The degree of shunting increased as CdTe thickness was reduced, and many cells were shorted completely. The shunt conductance of baseline cells is typically 1 mS-cm^2 and increased to >20 mS-cm^2 for 1 μm CdTe.

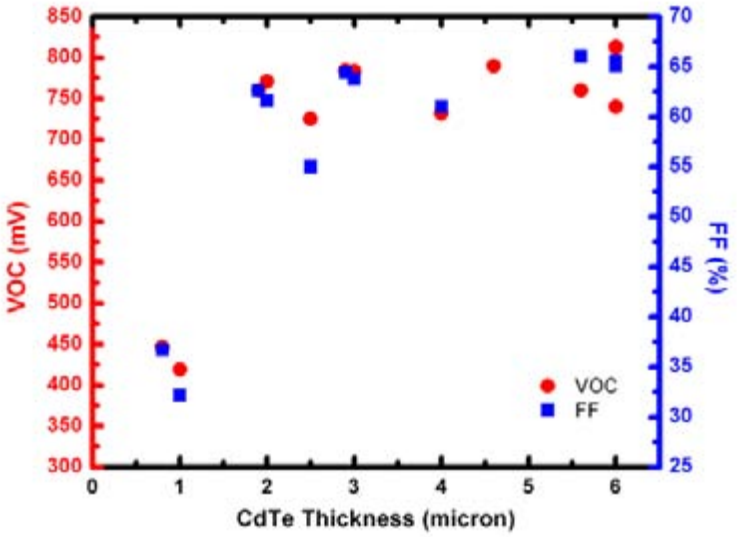

Figure 5. V_{OC} (red circles, left axis) and FF (blue squares, right axis) of CdS/CdTe cells processed with 2 min $CdCl_2$ treatment and BDH etch.

A milder surface etch using bromine-methanol (BrMeOH) yielded demonstrable improvement in device yield and tolerance to thinner absorber layers. Fig. 6 shows V_{OC} and FF of cells obtained with thin VT CdTe absorbers using the $CdCl_2$ protocols of Table IV with 2 minute treatments and BrMeOH etch. Baseline V_{OC} is retained down to an absorber thickness of 1.5 μm and follows a monotonic falloff thereafter. The best FF obtained with the BrMeOH etch is comparable to that achieved with the BDH etch but drops progressively with reduced CdTe thickness. However, the FF on cells using the BrMeOH etch are not dominated by shunt conductance. The area yield of cells processed with vapor treatment and mild BrMeOH approaches 100%, which verifies the low pinhole density and demonstrates the benign nature of this back contact process.

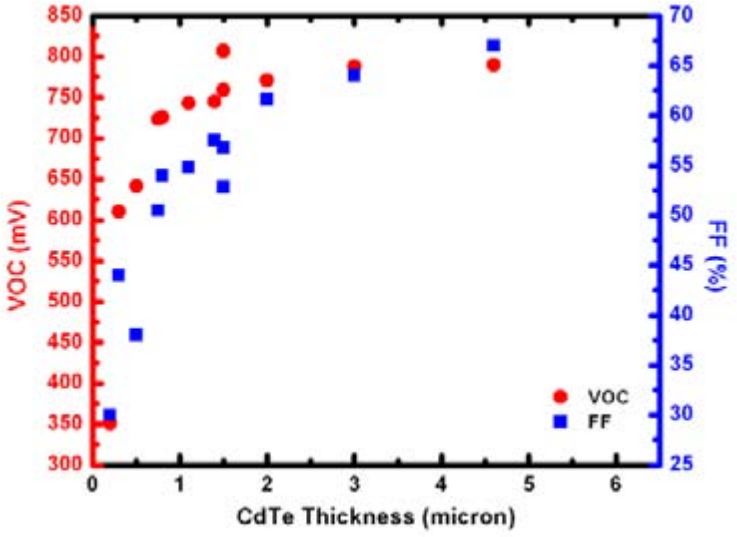

Figure 6. V_{OC} (red circles, left axis) and FF (blue squares, right axis) of CdS/CdTe cells processed with 2 min $CdCl_2$ treatment and BrMeOH etch.

The best cell results obtained for VT cells with thin CdTe absorber layers using 2 min vapor $CdCl_2$ treatment at 480°C and BrMeOH etching are listed in Table IV. The V_{OC} and FF decrease with reduced CdTe thickness, while J_{SC} remains relatively constant, dropping by ~1 mA/cm^2 for the cell with 0.8 μm thick CdTe.

Table IV. Best-cell J-V results for VT cells with thin CdTe absorber layers using vapor $CdCl_2$ treatment at 480ºC with 2 minute $CdCl_2$ time and etched with BrMeOH.

CdTe Thickness (μm)	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	η (%)
3.0	788	23.1	64.0	11.8
1.5	807	23.8	56.8	10.9
1.0	743	23.4	54.8	9.5
0.8	723	22.5	50.5	8.2

Some device sets, however, exhibit lower photocurrent than expected, based on the CdTe absorption data presented in the previous report (for January 2008 of this contract). The raw and normalized quantum efficiency (QE) of cells with thin CdTe are compared to a baseline cell (5 μm) in Figs. 7 and 8, respectively. The normalized data shows a shift in peak response towards the blue and the expected loss in the red. The raw data shows a 2X panchromatic loss not accounted for by decreased absorption, and QE measurements at reverse bias did not significantly improve collection. Thus, while the photo-response *profile* is attributable to optical absorption, the magnitude is related to photo-carrier collection. This behavior is correlated with the TEC15 glass batch, and more analysis is required to relate the behavior to glass impurities, effectiveness of the HRT layer as a diffusion barrier, and device processing.

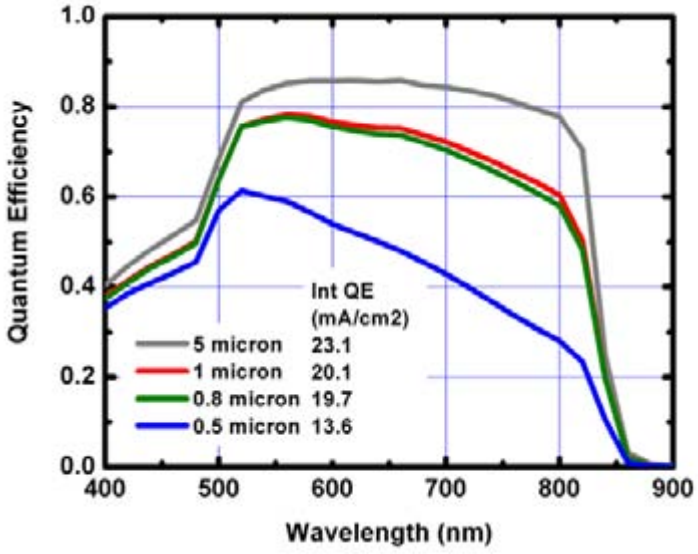

Figure 7. Raw QE (0V, light) of CdS/CdTe cells with baseline (top) and thin CdTe absorbers processed with 2 min $CdCl_2$ treatment.

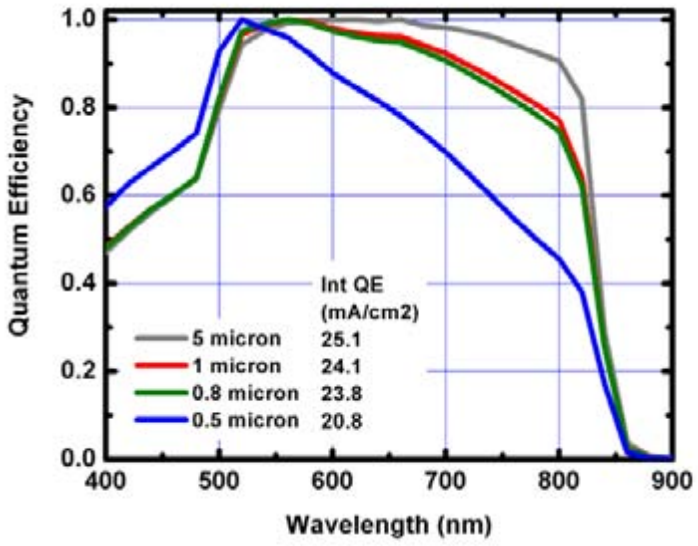

Figure 8. Normalized QE of CdS/CdTe cells with baseline (top) and thin CdTe absorbers of Figure 7.

Past x-ray diffraction and photoemission spectroscopic analyses of the surface of vapor $CdCl_2$ treated CdTe films showed the total oxide thickness to be <5 nm, suggesting the possibility of eliminating the etch step altogether for samples prepared with brief vapor $CdCl_2$ treatments. Cells with 3-5 μm CdTe fabricated with short vapor $CdCl_2$ treatment and no etch step yielded 12% conversion efficiencies.

Flexible CdTe Solar Cell

The goal of this sub-task is development of a process to deposit CdTe films in a superstrate configuration onto CdS/ITO window layers using a temporary Al foil substrate. Both low temperature PVD and high temperature VT deposition methods are considered for the CdTe film growth, allowing comparison of the mechanical and chemical robustness of films deposited at low temperature with those deposited at high temperature. The primary structural effect of deposition temperature is on grain size and structure. The PVD technique, with Ts < 400ºC, does not achieve the grain size and low crystallographic defect density found in films deposited at high temperature (Ts > 450ºC). However, the technique imparts the least thermal stress on the thin film and Al foil system.

A primary objective of this work is transferring the completed CdTe solar cell onto a polymer substrate, and the key challenges are selection of an appropriate bonding agent/substrate combination for mechanical robustness and low contact resistance and a chemical etchant for removing the Al substrate. Initial efforts were focused on single-sided adhesive Kapton tape and lamination directly onto polymer substrates using a conductive epoxy. On-going work is the fabrication and characterization of devices to determine: 1) the effect of the Al substrate on p-n junction behavior; 2) the effect of Al etching and etching on device operation; and 3) the mechanical effects of different

adhesion methods on the durability of the transferred solar cell. Backwall J-V analysis of partially-completed devices will be used to monitor the progress of junction quality through the post-deposition and transfer process. We anticipate future analysis of stress-induced effects on device operation, in view of the fact that cells will undergo stresses related to mechanical deployment and thermal cycling. The mechanical robustness of the CdTe solar cell transferred to a polymer substrate is an open question. Adhesion and mechanical strength will be characterized with respect to deformation caused by bending of the substrate. Adhesion will be quantified by standard tape tests. Mechanical strength of the structure will be determined by the minimum radius at which the on-set of cracking is detected. In this context, the issue of fatigue fracture will be also be evaluated.

Figure 9 shows a schematic representation of the transfer process of a CdTe/CdS thin-film device from the temporary Al superstrate to a flexible polymer substrate. The process steps used in preliminary experiments are:

1. Sputter 0.25-0.30 μm thick ITO film on 0.002 cm thick Al foil;
2. Evaporate 0.2 μm thick CdS film at 220ºC and 3 Å/s;
3. Evaporate 4.0 μm thick CdTe film at 340ºC and 30 Å/s;
4. Vapor treat structure in $CdCl_2$:Ar:O_2 ambient at 400ºC for 20 minutes;
5. Vapor treat back surface and deposit Cu to form cuprous telluride;
6. Evaporate Ni contact;
7. Bond cell to polymer substrate;
8. Etch Al foil in 1 molar NaOH at 35ºC.

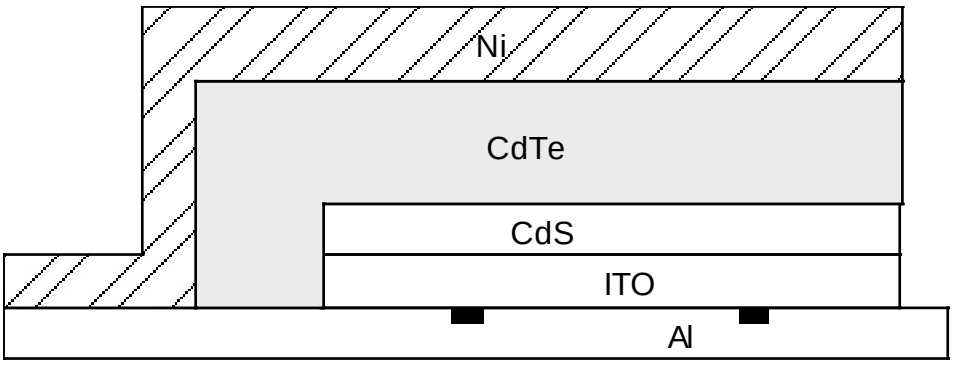

Figure 9a. As-deposited CdTe/CdS superstrate structure on Al foil.

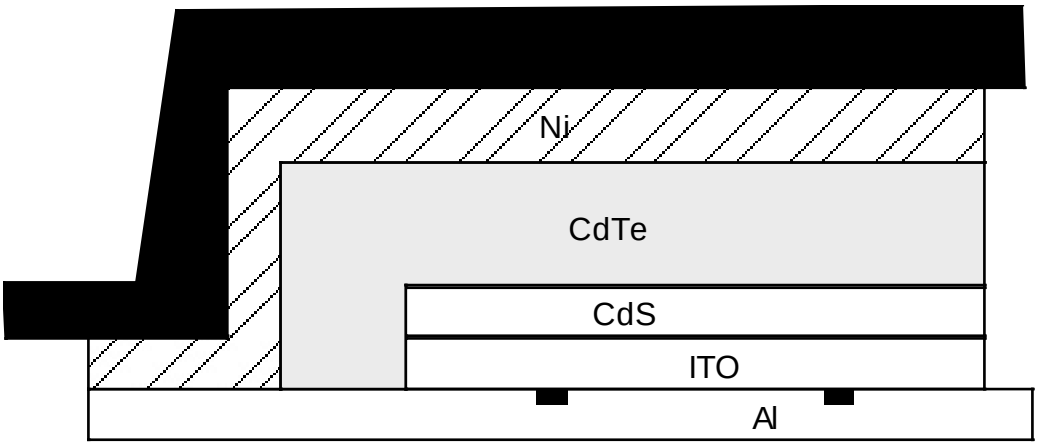

Figure 9b. Intermediate structure bonded to polymer material.

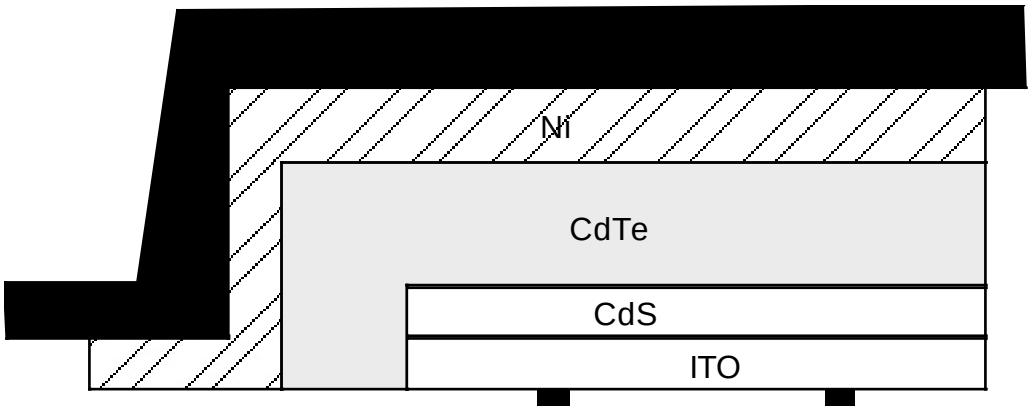

Figure 9c. Final CdTe/CdS device: Al foil temporary substrate etched away.

To support the Al foil throughout the deposition sequence, it was wrapped around a 10 cm x 10 cm stainless steel platen. Initially, soda lime glass was employed but was found to frequently crack during VT CdTe deposition or during cool-down. In all experiments, the CdS was deposited by PVD at 150°C at a growth rate of 5A/s. Figure 10 shows a photograph of the CdS-coated ITO/Al structure of 1" x 3" sections taken from a PVD and a VT run, each with nominally 4 μm thick CdTe.

Figure 10. As-deposited ITO/Al structure.

Figure 11. As-deposited CdS/ITO/Al structure.

Figure 12. CdTe/CdS/ITO/Al structures with CdTe deposited by PVD (left) and VT (right).

In a preliminary experiment, we transferred a completed 2 cm x 2 cm Ni/CdTe/CdS/ITO device with a 4 μm thick VT CdTe layer from an Al foil superstrate to Mo-coated Upilex polyimide sheet using a conductive silver epoxy. The temporary foil substrate used was 40 μm thick ultra-high vacuum Al foil supplied by All-Foils, Inc. and the epoxy was No. 40-3905RSI04 by Epoxies Etc. Prior to bonding to Upilex, the cell structure was subjected to the same processing conditions used to fabricate baseline 11% efficient (AM 1.5) solar cells. As neither gridding nor TCO area definition was used in the preliminary experiments, photoresponse measurements were made using point contacts. The structure is flexible, exhibits an open circuit photovoltage of 300 mV and exhibits a weak photocurrent. Cracks in the CdTe film were correlated with crease-like distortions in the Al foil superstrate. Techniques for handling the foil will need to be developed and analyzed to determine the influence of superstrate condition on mechanical integrity of the CdTe film.

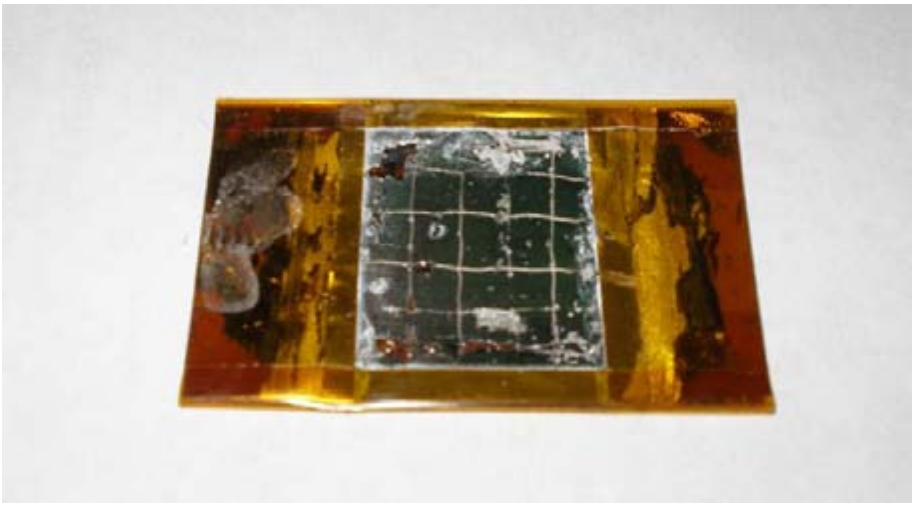

Figure 13. Transferred Ni/CdTe/CdS/ITO solar cell structure (3 cm x 2 cm) showing mechanical scribe lines to isolate smaller regions for electrical probing. Bright areas are regions where the CdTe cell delaminated from the silver epoxy during NaOH etching to remove Al.

Additional device structures were made using PVD CdS and VT CdTe films on ITO-coated Al foil superstrates. Cell transfer to flexible Upilex substrates was carried out using the same conductive Ag epoxy as reported in the previous report (for January 2008 of this contract). The temperature and strength of the NaOH bath needed to remove the Al was varied in an attempt to overcome the cracking phenomenon obtained for the conditions previously employed. The etch rate for Al foil was determined by measuring the time to completely etch 1 x 1 cm pieces in aqueous NaOH solution at different concentration and temperature. The etch rate results are listed in Table V.

Table V. Al foil etch rate for different NaOH solution concentration and temperature.

Temp (ºC) ± 1º C	NaOH:H_2O Strength (Molar)		
	0.1	**0.5**	**1**
	Etch rate (µm/min)		
30	0.29	0.73	0.85
40	0.45	1.50	1.86
50	0.74	1.85	2.48
60	1.26	3.79	4.97

Experiments with actual device structures were carried out at two extreme points in Table V: 0.1 Mol/30°C and 1 Mol/60°C. At 60°C, significant bubble formation at the edges caused undercutting of the device at the Ni/Ag epoxy interface, even after application of Kapton tape edge sealant. In addition, the Mo was damaged at the Mo/Upilex interface as a result of etching at regions of residual stress and oxidation (Mo grain surfaces), as a consequence of the Mo deposition conditions needed to deposit adherent Mo films on polyimide. At 30°C, the etch time was excessively long, and the entire structure was immersed in the bath for nearly an hour. In both cases, the transferred devices exhibit no detectable photoresponse. On-going effort is directed at evaluating alternative adhesives and mechanically robust and chemically inert back contact materials and configurations. In practice, transfer of PVD films was more robust then VT films. Backwall V_{OC} measurements after $CdCl_2$ treatment but prior to transfer gave $V_{OC} > 700$mV for both sample types. After transfer and removal of Al, $V_{OC} <$ 400mV was obtained. The results indicate that more work is needed to address mechanical and chemical issues of the transfer and that deposition of the cell onto Al superstrates does not degrade cell performance.

2.8 References

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3 $CuInSe_2$- BASED SOLAR CELLS

3.1 Phase 1 Summary: 9/5/01 to 9/4/02

In-line evaporation is a potentially effective means to achieve the high rate uniform deposition necessary for commercial-scale manufacture of $Cu(InGa)Se_2$ modules. Utilizing its unique in-line $Cu(InGa)Se_2$ evaporation system for deposition from stationary elemental sources onto a moving 6" wide substrate, IEC has developed a process to deposit $Cu(InGa)Se_2$ with good adhesion in a roll-to-roll process on flexible polyimide substrates. The polyimide substrate allows the potential advantages of roll-to-roll processing and fabrication into monolithically interconnected modules. With the flexible polyimide substrate, good adhesion between the Mo and $Cu(InGa)Se_2$ film was found to be a critical issue. This was achieved with a two step deposition process which included a Ga-In-Se precursor layer deposited on the polyimide/Mo web followed by deposition of the bulk of the $Cu(InGa)Se_2$ film. The materials properties of the $Cu(InGa)Se_2$ films were characterized along and across the web. Thickness and composition are uniform within measurement error and larger variations were found from deposition to deposition. Average device performance over a five-foot length was between 8 to 9% and the best cell, with the addition of a MgF_2 anti-reflection layer, had an efficiency of 12.1%

Substrate speed and temperature are particularly important process parameters, which have a direct impact on the manufacturing cost and process yield, particularly since the temperature of the polyimide substrates are limited to 450°C. Measurement and control of the polyimide substrate temperature during $Cu(InGa)Se_2$ deposition is difficult because of the small thermal mass of the web and the inability to attach a thermocouple for temperature measurement. To enable better control, a radiative model was developed for the substrate temperature and how it is coupled to both the substrate heater and the evaporation sources.

Increased V_{oc} for improved module performance

Increased V_{oc} in $Cu(InGa)Se_2$ devices is desirable because it should improve the performance of $CuInSe_2$-based modules. The approach to increasing V_{oc} is to increase the bandgap, Eg, in the absorber layer or in the space charge region by alloying the $CuInSe_2$ with Al or S. Previous work at IEC on $Cu(InAl)Se_2$ demonstrated that this material could be used as a wider bandgap alloy, but the solar cell efficiency was limited by poor adhesion between the Mo and $Cu(InAl)Se_2$ which limited the substrate temperature to $\leq$ 450°C. In this phase, a process was developed which improved adhesion, allowing the substrate temperature to be increased from 450 to 530°C during evaporation. This process utilizes a 5 nm thick Ga layer between the Mo back contact and the $Cu(InAl)Se_2$ film. $Cu(InAl)Se_2$ thin films have been deposited by elemental co-evaporation and solar cells with efficiency as high as 16.9% were demonstrated. The $Cu(InAl)Se_2$ band gap was varied from 1.1 to 1.7 eV by increasing Al/(In+Al) from 0 to 0.5 and the effect on material and device properties is presented. It was found that

$Cu(InAl)Se_2$ cells with band gaps greater than 1.5 eV have comparable efficiencies to the best cells using other wide band gap chalcopyrite alloys. The effects of the increase in substrate temperature on the films and devices were also characterized.

The partial replacement of Se with S in the surface region of $Cu(InGa)Se_2$ films can also be used to increase V_{oc}. Optimization of this effect requires a quantitative understanding of the S incorporation process into the absorber layer. In thin films both bulk and grain boundary diffusion must be considered. For S reaction with $CuInSe_2$ films that are slightly Cu rich, a model assuming constant diffusion coefficients has been previously developed. In sulfurization experiments on films, which were slightly Cu deficient, smaller values of the diffusion coefficient, were found and could not be analyzed by the simple diffusion model. The results suggested that the diffusion coefficient could be concentration dependent. Experiments to separate the effects of the bulk and grain boundary diffusion and of a second Cu-Se phase are currently being developed.

Atomic level surface and interface characterization

A more fundamental understanding of $Cu(InGa)Se_2$ solar cells will require characterization of the critical surfaces and interfaces in the devices. IEC has begun to address some of the issues related to surfaces and interfaces using atomic level surface characterization and device characterization techniques. In this phase, effort has focussed on two areas. The first has been to develop the capability to deposit ZnS and CdZnS buffer layers using chemical bath deposition methods. This will be used to study the effect of the $Cu(InGa)Se_2$/buffer layer interface chemistry and band alignment on devices. A process for chemical bath deposition of ZnS from solutions of $ZnSO_4$, thiourea and ammonia was developed. The bath conditions and concentrations were optimized to deposit homogeneous microcrystalline films with 3.6 eV bandgap and good coverage on all substrates. $Cu(InGa)Se_2$ solar cells fabricated with the ZnS buffer had higher quantum efficiency at short wavelengths but V_{oc} and FF were a little lower than those with CdS buffer. The best cell with the ZnS buffer had 13.9% efficiency. CdZnS films have also been deposited by chemical bath deposition. Comparable cell performance was obtained with CdS or CdZnS.

The second area of focus has been $Cu(InGa)Se_2$ surface characterization to quantitatively analyze the accumulation of Na on the surface and diffusion from the glass substrate. The Na diffusion was found to depend on the atmosphere in which samples were annealed, with Na accumulating on the $Cu(InGa)Se_2$ surface after anneals in O_2 or air, but not in vacuum. Also the Na accumulation depended on the previous history of the sample with the surface concentration decreasing after successive cycles of cleaning the surface and annealing. Finally, the apparent activation energy for Na diffusion through the Mo and $Cu(InGa)Se_2$ was determined from the surface concentrations after anneals at different temperatures.

Cu(InGa)Se2 TFP Team Activity and Collaboration

IEC fabricated complete solar cells and completed JV and QE measurements and analysis on a set of absorber layers provided by 5 different members of the Absorber Sub-team for the CIS Team of the Thin Film PV Partnership. This set included 3-4 samples each from EPV, GSE, ISET, NREL, and SSI. Details and results are presented in the National CIS R&D Team Minutes of the meeting at New Orleans on May 19, 2002.

3.2 Phase 2 Summary: 9/5/02 to 9/4/03

Development of the roll-to-roll deposition of CIGS on polyimide web focused on film cracking and / low adhesion with specific effort on finding a correlation with the Mo deposition process. Mo films were deposited onto two types of Upilex (S and SG) with and without oxygen plasma treatment and at different temperatures and gas pressures but CIGS film cracking and adhesion were found to be insensitive to these variations. A number of changes were made to the CIGS roll-to-roll deposition system to improve its robustness and reproductibility. In this respect, a new Se source design now allows the control of the surface temperature of the liquid Se source. Shielding of the thermocouple extension wires made possible the temperature control of the source effusion rates, which is more robust than the Atomic Absorption Spectroscopy control.

Work on CIS-based devices with increased V_{OC} focused on adhesion and material and device performance of Al containing alloys, and on S diffusion into CIS and CIGS films. Al alloy films have been deposited by 1-step (constant flux), 2-step (Al-rich flux followed by Cu-free flux), and 3-step (Cu-free flux at low temperatures followed by only Cu flux and then Cu-free flux at higher temperatures processes. Going from 1-step to 3-step processes grain size was found to increase. Film adhesion was similar for 1-step and 2-step processes, but much worse for the films prepared by the 3-step process. Device results showed similar efficiencies for 1-step and 2-step processes, decreasing with increasing Al content. Films prepared by the 3-step process could not be made into devices except for the lowest Al content films due to the poor adhesion. QE data showed increasing voltage dependent collection with increasing Al content, i.e. increasing bandgap.

Characterization of the physical vapor deposited films on Cu, Al and Se to form the ternary $CuAlSe_2$ showed different structure depending on the ratio of Se flux R_{SE} to total metal flux R_M. R_{SE}/R_M <10 gives mixed phases of Cu-Al inter-metallic phases plus Al_2Se_3 to $CuAlSe_2$ + Cu_2Se going through single-phase $CuAlSe_2$ depending on the Cu/Al ratio. For R_{SE}/R_M >10 the structure is a mixture of $CuAlSe_2$ and a new phase β-$CuAlSe_2$.

In the area of fundamental studies, alternative emitter layer materials and processes were evaluated and optical properties and electronic transitions in $Cu(InGa)Se_2$ films were determined through spectroscopic ellipsometry. Air annealed chemical bath deposited ZnS films to form mixed sulfide-oxide layers were characterized both optically and structurally. While bandgap decreases with air anneal intensity, glancing angle incidence

XRD does not indicate any sulfide-oxide alloy formation. Devices made with the ZnS window layer do not show any correlation between efficiency and air-anneal time. CdS layers formed by chemical surface deposition method were evaluated for their potential in $Cu(InGa)Se_2$ based devices. The process is highly desirable from a manufacturing point of view, since it has high utilization rate and low waste; devices made with CdS deposited by this process demonstrated high efficiencies showing the expected promise.

Optical constants of polycrystalline thin film $CuIn_{1-x}Ga_xSe_2$ alloys with Ga/(Ga+In) ratios from 0 to 1 have been determined by spectroscopic ellipsometry over an energy range from 0.75 to 4.6eV. $CuIn_{1-x}Ga_xSe_2$ films were deposited by simultaneous thermal evaporation of elemental copper, indium, gallium and selenium. X-ray diffraction measurements show that the $CuIn_{1-x}Ga_xSe_2$ films are single phase. Due to their high surface roughness, the films are generally not suitable for ellipsometer measurements. An innovative method was developed in which spectroscopic ellipsometer measurements were carried out on the reverse side of the $CuIn_{1-x}Ga_xSe_2$ Films immediately after peeling them from the Mo-coated soda lime glass substrates. A detailed description of multilayer optical modeling of ellipsometric data, generic to ternary chalcopyrite films, is presented. Accurate values of the refractive index and extinction coefficient were obtained and the effects of varying Ga concentration on the electronic transition were determined.

CIGS TFP Team Activity and Collaboration

IEC attended the National CIS R&D Team meeting on January 30-31, 2003 and participated in work by the Absorber Sub-team. We presented a review titled "Status of Wide Bandgap $CuInSe_2$-based Solar Cells". Additional team-related activity and collaboration included:

- $Cu(InGa)Se_2$ samples deposited at either 400°C or 550°C using either a uniform or bi-layer (Cu-rich at start) deposition process were provided to the University of Illinois for TEM characterization. A set of well characterized $Cu(InGa)Se_2$ films were also provided to UI for EDS standards.

- IEC fabricated devices on a set of 12 $Cu(InGa)S_2$ films from Florida Solar Energy Center and completed J-V and QE measurements to assist FSEC in evaluating it's absorber layer and device fabrication processes.

- Optical constants measured by spectroscopic ellipsometry as a function of energy of $Cu(InGa)Se_2$ with different relative Ga content were sent to several team members for input into their modeling efforts.

- CdS and ZnO/ITO depositions were completed on several sets of samples, in a round-robin experiment with GSE and NREL, to use for characterization of GSE's device processing and calibration of their emitter and TCO layer thicknesses.

- Collaboration with the University of Oregon on device characterization continued with focus on Cu(InAl)Se_2 devices with different bandgaps for comparison to previously characterized Cu(InGa)Se_2 devices.

3.3 Phase 3 Summary: 9/5/03 to 9/4/04

The process for the roll-to-roll deposition of Cu(InGa)Se_2 on polymer substrate has been improved during the past year by developing several system improvements and reducing or eliminating the cracking of the Mo back contact film in the Cu(InGa)Se_2 reactor. The system was made more robust and stable with a new evaporation source design and improved Se delivery system. The new Cu source has a design, which avoids sharp internal lines and corners that acted as stress concentrators. In addition, the design includes conical nozzles that eliminated spitting of Cu droplets and allows higher rate deposition. The Se delivery manifold was simplified and reduced to a single 3/8" stainless steel tube with two effusion holes. A larger Se source was designed and implemented which incorporates improved ability to measure and control the melt temperature as well as greater capacity. Cracking of the Mo film on polyimide substrates after Cu(InGa)Se_2 deposition has been a significant problem hampering progress with the roll-to-roll flexible Cu(InGa)Se_2. The extent of film cracking was reduced with lower excess Se flux in the reactor implying that reaction of the Mo back-contact with Se was responsible for crack formation by reducing the yield strength of the Mo film. Since Mo oxides are more stable than the selenides, Mo films were prepared containing around 8 at% oxygen by sputtering in a mixed Ar/O_2 atmosphere. It was thought that introducing controlled oxygen content into the Mo film could reduce reaction with Se and thus eliminate cracking. Based on this line of logic. These films did not show any cracks, as evidenced by microscopic characterization and by device performance, indicating that the oxygenated Mo had reduced reaction with Se to prevent cracking. With these changes to the system and substrate, improved deposition reproducibility and compositional and device uniformity was demonstrated.

Diffusion of sulfur into Cu(InGa)Se_2 thin films could provide a means to increase V_{OC} by widening the bandgap in the space charge region of the absorber. A fundamental study of the mechanisms of S-diffusion was completed using reaction of thin films and crystals in H_2S. Two modes of S incorporation in the $CuInSe_2$ were distinguished. Rapid S incorporation with a breakdown of the crystal lattice occurred in materials containing excess Cu. In single-phase films or crystals, a slow S incorporation was observed. Quantitative models of the S-diffusion and diffusion coefficients were developed for these two cases. Also, S was incorporated into evaporated $CuInSe_2$ and Cu(InGa)Se_2 films by annealing them in diluted hydrogen sulfide combined with oxygen and hydrogen selenide. After reaction in H_2S or H_2S combined with O_2, a fully converted sulfide layer was formed at the surface of the absorber layer, which would create a barrier for current collection in devices. A mixed hydride gas H_2S + H_2Se a graded Cu(InGa)$(SeS)_2$ layer on the top of the absorber layer was formed and at the same time the Ga diffuses away from the surface. Thus, the bandgap in the near surface region could not be controllably

increased with S diffusion so it does not appear to be a promising avenue for increased V_{OC}.

Research on $CuInSe_2$-based devices with increased V_{OC} has focused on determining the cause for poor adhesion which has limited the ability to fabricate wide bandgap $Cu(InAl)Se_2$ devices, and on S-diffusion in $Cu(InGa)Se_2$ for widening the bandgap in the near surface region. Poor adhesion at the Mo/$Cu(InAl)Se_2$ interface was identified as a critical issue and was previously improved by incorporating a thin, ~ 5 nm, Ga layer sputtered onto the Mo film prior to the $Cu(InAl)Se_2$ deposition. Still, devices with increasing bandgap or using different deposition processes were severely hampered by poor Mo/$Cu(InAl)Se_2$ adhesion. Poor adhesion at the Mo interface can also be problematic for the fabrication of $Cu(InGa)Se_2$ cells on flexible polyimide substrates. Research is focused on determining how Ga and/or Al at the Mo interface affects the formation and orientation of a $MoSe_2$ interlayer. The $MoSe_2$ forms a layered structure and orientation of these layers parallel to the substrate can lead to poor adhesion. Mo, Mo/Cu and Mo/Ga layers were reacted with Se and x-ray diffraction measurements showed that the $MoSe_2$ had a more preferred orientation with Ga than with Cu. Similar experiments with Al could not be completed since it was limited by the formation of Al_2O_3 or, with Mo/Cu/Al layers, formation of Cu-Al intermetallic compounds. A second method was to characterize the $MoSe_2$ after peeling off the $CuInSe_2$-based films but the remaining layers were found to be unstable.

Fundamental characterization of the optical properties of $Cu(InGa)Se_2$ continued. Previously, a method to determine optical constants of $Cu(InGa)Se_2$ films using spectroscopic ellipsometry (SE) was developed and variation with Ga/(Ga+In) ratios from 0 to 1 was determined. In this phase, we have focused on the effect of Cu stoichiometry in Cu-poor materials since high efficiency devices are made using single or two-phase Cu-poor films. For both Cu-In-Se and Cu-In-Ga-Se alloy films, an optical model was developed which allows the optical constants of mixed phase materials to be described by a mixture of the single phases, $CuInSe_2$ and $CuIn_3Se_5$ for the ternary case. Complete determination of the optical constants for films with Cu at. % from 11 to 25 % was completed. This enables the composition of the mixed phase materials to be determined using the SE measurements. For each alloy system, there is an increase in the energy of the lowest order transitions, which determine the bandgap. Also, there is a broadening of critical point feature, which indicated decreasing crystalline quality.

The effect of the $Cu(InGa)Se_2$/emitter layer interface and band alignment on devices is being studied by changing the alloy compositions of the $Cu(InGa)Se_2$ layers and using CdS, (CdZn)S or ZnS emitter layers. Also, chemical bath (CBD) and high utilization chemical surface (CSD) depositions were compared. A process for CSD (CdZn)S was developed and increased bandgap with Zn addition was confirmed by QE measurements. In all cases, the (CdZn)S gave comparable performance to the CdS emitter layer with both 1.2 and 1.4 – 1.5 eV absorber layer bandgaps. The ZnS emitter layers gave poor device efficiency. The CSD process resulted in ~30 mV lower V_{OC} than the CBD process which was not improved with an ammonia surface treatment prior to CdS

deposition similar to the first step in the CBD process, indicating the complexity of the interface chemistry in controlling device behavior.

Cu(InGa)Se2 TFP Team activities and collaboration

IEC activities in support of the $CuInSe_2$ National Team and other research groups working on $CuInSe_2$ development have included the following:

Thin Film Partnership $CuInSe_2$ National Team: IEC has collaborated with several members of the Absorber Sub-Team to complete a study comparing characterization of films and devices from 6 different groups. In particular, IEC completed analysis of J-V and QE data on devices it had previously fabricated using different $Cu(InGa)(SeS)_2$ absorber layers.

University of Illinois: $Cu(InGa)Se_2$ samples were provided to the U. of Illinois for TEM and other microstructural analysis. Specific samples included films deposited at different temperatures, comparing uniform flux, two-step, and three-step processes, and deposited on Na-free glass for comparison to films grown with Na diffusion from the soda lime glass substrate.

University of Oregon: IEC continued its collaboration with the University of Oregon in the analysis of $Cu(InGa)Se_2$ based devices. Specifically, IEC has provided various devices using different absorber layers and substrates.

Miasole: IEC fabricated solar cells and completed JV and QE measurements to help Miasole characterize their $Cu(InGa)Se_2$ deposition process.

InterPhases Research: IEC completed cell fabrication and provided J-V testing on a set of samples from InterPhases Research to test their novel surface treatments. In addition, IEC has provided glass/Mo/$Cu(InGa)Se_2$ films for treatment

3.4 Phase 4 Summary: 9/5/04 to 9/4/05

Research on $CuInSe_2$-based solar cells includes four different tasks: (1) In-Line Evaporation; (2) Wide Bandgap Materials; (3) $Cu(InGa)(SeS)_2$ Formation by H_2Se/H_2S Reaction; and (4) Fundamental Materials and Interface Characterization. In each case, significant progress has been made, as documented in this report.

The development of the process of in-line deposition of $Cu(InGa)Se_2$ on polymer substrates focused on the linear metal evaporation sources and on the preliminary investigation on the understanding of the role of oxygen in Mo back contact in preventing film cracking. The insulation of the 6" metal sources that are presently in use has been entirely modified, switching over to rigid alumina boards. In parallel with this change, all the carbon/graphite-based components in the source have been replaced to eliminate

reaction with metallic parts, such as thermocouples and Ta shields. These changes enabled operation of the sources at lower temperatures. The problem of metal vapors leaking between the lid and the source body was also addressed. A sealed source was designed and fabricated. This new source will be tested in the near future. The instability of the Cu source power control at high temperature was finally traced to the multi-channel thermocouple interface module which generated a noisy signal for C-type thermocouple when the signal gets to be higher than 20mV and that there are other thermocouples connected to other channels. The temporary solution, connecting the Cu source thermocouple to its own interface module, allowed system operation without any control problem. In addition, issues associated with the sources in scaling-up the in-line deposition to 13" web were investigated. A bell-jar system with a single source was set-up to determine and analyze the temperature distribution on the present 6" source. Further, simulation of the temperature distribution on a 13" system was performed. The comparison showed that simple scale-up of present sources, which give adequate film uniformity, would result unacceptable non-uniformities over the 13" wide web. Consequently, a number of design options to overcome this problem were evaluated. The issues related to source depletion over long runs, resulting in thermal characteristics leading to drifts in the effusion rates, were also examined. As to the role of oxygen in preventing the Mo back contact film cracking, the Auger depth profiling analysis shed more light to the problem. Comparison of the profiles before and after the $Cu(InGa)Se_2$ deposition showed that there is a diffusional rearrangement of oxygen in the Mo layer, resulting in a uniform distribution, irrespective of the initial oxygen distribution in the Mo film. This point will be further pursued in the coming year.

Work on wide bandgap materials remained focused on $Cu(InAl)Se_2$ films deposited by multisource elemental co-evaporation. The primary problems being addressed are poor reproducibility, partly caused by poor adhesion at the Mo/$Cu(InAl)Se_2$ interface, and poor performance with low V_{oc} as the bandgap is increased. Progress is reported in this report on developing alternative evaporation sequences, characterizing the back contact, and gaining a more complete understanding of the basic material properties. A simplified continuous version of a three-stage evaporation process was developed and end-point detection of the substrate temperature was used to control the film composition. Films were grown with different relative Al contents material. As Al content increased, the grain size decreased, adhesion worsened, and device performance got much worse. The variation in material and device properties as a function of Cu off-stoichiometry was also studied. Formation of an ordered vacancy chalcopyrite structure with low Cu content was verified. Devices with this compound had poor device performance and an ~ 0.2 eV shift in the long-wavelength QE, indicating a shift in bandgap.

Critical issues for the formation of $Cu(InGa)(SeS)_2$ films by the selenization or sulfization reactions of Cu-Ga-In precursor films have been investigated. A complete understanding of the reaction process requires characterizing phases in the as-deposited precursor films, and after annealing with different time-temperature-gas concentration profiles used to control the reaction pathway. Metal precursor films were deposited by sputtering a Cu-Ga layer from a $Cu_{0.8}Ga_{0.2}$ alloy target, followed by an In layer. The phases present in the sputtered metal precursors after annealing at 450°C were Cu, In,

CuIn and $Cu_9(In_{1-x}Ga_x)_4$. Films reacted in hydrogen selenide (H_2Se) or hydrogen sulfide (H_2S) were characterized and unreacted intermetallic Cu-Ga or Cu-In phases respectively were identified at the back of the films. This indicates a reaction preference of Se with In, and S with Ga. Homogenization of the Ga using a two-step selenization/sulfization process that takes advantage of this reaction preference was confirmed, and different time-temperature profiles were compared. Devices with $V_{oc} > 0.64$ V and eff. > 13% were demonstrated. With a better understanding of the reaction pathway, work will be focused on optimization of the time-temperature sequence of the two-step reaction to better understand the mechanism for Ga mobility to control the S composition at the front of the film, and ultimately, to improve device performance.

Fundamental characterization of materials and interfaces has largely focused on a detailed characterization of the optical properties of $Cu(InGa)Se_2$ thin films as a function of changes in composition, including variations in the relative gallium and copper concentrations. The characterization was done using variable angle spectroscopic ellipsometry with a novel technique developed previously at IEC, in which the $Cu(InGa)Se_2$ is lifted off the glass/Mo substrate to provide access to a smooth surface for optical characterization. The complex optical constants and critical transition energies of $Cu(InGa)Se_2$ were previously determined for films varying in relative gallium content spanning from $CuInSe_2$ to $CuGaSe_2$. Since all $Cu(InGa)Se_2$ solar cells are made using Cu-deficient films, it is valuable to relate the optical properties to the degree of Cu off-stoichiometry. A method has been developed to determine the optical constants of films with decreasing Cu content in the Cu-deficient two-phase region as a mixture of the optical properties of the single-phase endpoints with high and low Cu concentrations. The decrease in Cu is characterized by an increase in the fundamental bandgap and broadening of critical point features in the optical constants suggesting degradation of the crystalline quality of the material. This optical analysis can be used to determine the volume fraction of these two phases, which directly determines the film composition.

An aqueous Br-etch has been used for smoothing $Cu(InGa)Se_2$ films to obtain a specular surface for optical modeling and interface characterization. The etch also controllably reduces the $Cu(InGa)Se_2$ thickness to study device behavior with thin absorbers and enable characterization of the Mo/$Cu(InGa)Se_2$ interface. The etch procedure was optimized to give the smoothest surface and controllable etch rates. Determination of $Cu(InGa)Se_2$ optical constants using the etch surface or the smooth surface obtained by peeling the films from the Mo contact gave comparable results so the etch does not seem not change the bulk $Cu(InGa)Se_2$. Devices fabricated after etching for different times had lower J_{sc} due to increased reflectivity with the specular surface and a lower V_{oc} that is not understood. Further efforts will be used to characterize the effects of $Cu(InGa)Se_2$ thickness and the back contact.

Research has also focused on the $Cu(InGa)Se_2$/CdS interface. High utilization chemical surface deposition was compared to chemical bath deposition, and it was shown that, under well controlled conditions, the same average device performance could be obtained. Also, optical constants of the CdS grown by chemical bath deposition were

measured directly on $Cu(InGa)Se_2$, using ellipsometry and showed broad optical transition consistent with poor crystallinity.

Cu(InGa)Se2 TFP Team Activity and Collaboration

IEC activities in support of the $CuInSe_2$ National Team and other research groups working on $Cu(InGa)Se_2$ development have included the following:

Thin Film Partnership – $CuInSe_2$ National Team
IEC attended the $CuInSe_2$ National Team meeting on March 8, 2005 and gave a presentation titled "$Cu(InGa)Se_2$ processing research at IEC: Composition control during selenization."

IEC also continued its ongoing collaboration with team members in the characterization of $Cu(InGa)Se_2$ films and devices from different groups. This work has resulted in the paper: "Comparison of device performance and measured transport parameters in widely-varying $Cu(In,Ga)(Se,S)_2$ solar cells" by I. L. Repins, B. J. Stanbery, D. L. Young, S. S. Li, W. K. Metzger, C. L. Perkins, W. N. Shafarman, M. E. Beck, L. Chen, V. K. Kapur, D. Tarrant, M. D. Gonzalez, D. G. Jensen, T. J. Anderson, X. Wang, L. L. Kerr, B. Keyes, S. Asher, A. Delahoy, B. Von Roedern, published in *Progress in Photovoltaics.*

Energy Photovoltaics
IEC has collaborated with EPV on alternative back contacts. In particular, IEC has fabricated and characterized devices using alternative back contacts deposited by EPV, which should provide improved reflectivity for devices with thin $Cu(InGa)Se_2$ absorbers. In addition, IEC has collaborated with EPV on evaporation source design and provided a design for a laboratory scale Cu evaporation source.

ISET
IEC has assisted ISET in the characterization of series resistance in devices and the design of collection grids for solar cells. In addition, IEC provided Mo-coated polyamide substrates for fabrication of flexible $Cu(InGa)Se_2$ solar cells.

University of Illinois
IEC has provided samples for novel characterization at University of Illinois This includes structural characterization using high resolution TEM techniques and Near Field Scanning Optical Microscopy (NSOM) measurements. This work has resulted in a paper "Application of Advanced Microstructural and Microchemical Microscopy Techniques to Chalcopyrite Solar Cells," C. Lei, C.M. Li, A. Rockett, I.M. Robertson and W.N. Shafarman, Mat. Res. Soc. Symp. Proc., (2005) *In press.*

University of Oregon
IEC has continued its ongoing collaboration with the U. of Oregon to characterize electronic properties of $Cu(InGa)Se_2$ solar cells. In the past year this has resulted in two publications: "Detailed Study of Metastable Effects in the $Cu(InGa)Se_2$ Alloys: Test of Defect Creation Models," J.W. Lee, J.T. Heath, J.D. Cohen and W.N. Shafarman, Mat.

Res. Soc. Symp. Proc. **865**, 373 (2005), and "Defect Studies Using Photocapacitance Spectroscopy in the Copper Indium Diselenide Alloys," J.D. Cohen, J.T. Heath and W.N. Shafarman, Chapter 13 in Wide Gap Chalcopyrites, ed. by U. Rau S. Siebentritt (Springer Scientific, 2005) *In press*.

3.5 Phase 5 Summary: 9/5/05 to 3/31/07

Efforts on $CuInSe_2$-based solar cells include work on four different topics: (1) $Cu(InGa)(SeS)_2$ formation by H_2Se/H_2S reaction; (2) wide bandgap materials; (3) reduced thickness for $Cu(InGa)Se_2$ absorber layers; and (4) characterization of the $Mo/Cu(InGa)(SeS)_2$ contact.

The two-reaction selenization/sulfization of metallic Cu-In-Ga precursors is a commercially viable process for the manufacture of $Cu(InGa)(SeS)_2$ films. A two-step process with partial reaction in H_2Se followed by higher temperature reaction in H_2S has been shown to produce films with controlled incorporation of Ga. This enables higher bandgap in the active region of the film and higher V_{OC} in devices. In this report, results are included in three aspects of the characterization of $Cu(InGa)(SeS)_2$ formation by the reaction of Cu-Ga-In precursors: characterization of the metallic precursor layers; characterization of lateral non-uniformities in the reacted films; and results with the two-step H_2Se/H_2S reaction for films with homogeneous [Ga]/[In+Ga] profiles.

Metal precursor films were deposited by sputtering a Cu-Ga layer from a Cu0.8Ga0.2 alloy target, followed by an In layer or by sequential Cu, Ga, and In layers. The two precursor structures have different intermetallic phases and morphology in the as-deposited state but after annealing at 450°C, they contain the same mixture of a $Cu_9(In0.64Ga0.36)_4$ intermetallic phase and In. A frequent occurrence in the $Cu(InGa)(SeS)_2$ formation by 2-step reaction in H_2Se/H_2S is the development of lateral non-uniformities in the reacted films. These have been reduced by annealing the precursors to homogenize the phase composition prior to hydride reaction and by improving the uniformity of the heating in the reactor. However, non-uniformities near the sample edges remain and may be caused by a non-uniform Na diffusion. To characterize the two-step H_2Se/H_2S reaction process, a 2 x 2 matrix of reaction times was examined. Samples were selenized for either 15 or 30 minutes at 450ºC, followed by sulfization at 550ºC for either 15 or 30 minutes. Samples partially selenized for 15 minutes exhibited uniform Ga through the depth of the film after H2S reaction, but those more fully reacted in H2Se for 30 minutes exhibited the commonly observed back-contact Ga accumulation after H_2S reaction. In all cases, the S is largely accumulated near the front surface.

Work on wide bandgap materials remained focused on $Cu(InAl)Se_2$ films deposited by multisource elemental co-evaporation. Recent efforts on $Cu(InAl)Se_2$ have focused on developing alternative evaporation sequences and a more complete understanding of fundamental material properties.. Variations in the substrate temperature and composition of films deposited with a modified 3-stage process discussed have been used to characterize the properties of the $Cu(InAl)Se_2$ surface. The formation of a

$Cu(InAl)_2Se3.5$ ordered vacancy phase (OVC) phase forms as a surface layer, similar to that found at the surface of $Cu(InGa)Se_2$ films. However, there is no apparent effect of this layer on the device performance.

The effects of reducing the thickness of the $Cu(InGa)Se_2$ absorber layer below 1 μm have been studied using an aqueous Br-etch to smooth the surface of $Cu(InGa)Se_2$ films and reduce their thickness. $Cu(InGa)Se_2$ films with uniform through-film composition were etched for different times to vary thickness from 1.8 to 0.4 μm. Solar cells were fabricated with the etched films and with films deposited for different times to vary the thickness. Devices had fill factor greater than 74% over the entire range and little loss in V_{OC}, indicating no change in the critical electronic properties of the devices. The main loss in efficiency with thickness less than 1 μm is from lower short circuit current due partly to incomplete optical absorption but greater than predicted by models.

Research has also focused on the Mo/$Cu(InGa)(SeS)_2$ interface since the formation of a $MoSe_2$ layer at the back contact between Mo and $Cu(InGa)(SeS)_2$ can be a source of adhesion problems. Experiments have been done to characterize the reaction of Mo with H_2Se and H_2S to understand the back contact formation in the process of forming $Cu(InGa)(SeS)_2$ with reaction in the hydride gases. Sputtered Mo films on soda lime glass substrates were reacted for 1 hour in flowing H_2Se, H_2S, or an equal mixture of the two. XRD and XPS measurements show the formation of $MoSe_2$ at the surface of the films reacted in H_2Se or mixed gases and MoS_2 only for the film reacted in pure H_2S even though the heats of formation favor MoS_2 over $MoSe_2$. The interface between the Mo and evaporated $CuIn(SeS)_2$ was also characterized by lifting off the chalcopyrite layer. In this case, the interface layer contained much more S than Se, indicating a preference for the reaction of Mo with S.

CIGS TFP Team Activity and Collaboration

IEC has collaborated with, or provided assistance to, several other university and industrial groups working on $Cu(InGa)Se_2$ solar cells in the past year. These include:

<u>Ascent Solar, DayStar, HelioVolt, Miasolé, Nanosolar, SoloPower, Solyndra</u>

IEC has leveraged its expertise, baseline processes, and characterization facilities to assist these companies in a variety of ways, including: reacting precursor films to form $Cu(InGa)(SeS)_2$ and characterizing the resulting materials. fabricating cells to validate their cell fabrication processes.

Case Western Reserve University

IEC provided Cu(InGa)Se_2 samples with different compositions and deposited on different substrates for TEM analysis.

Energy Photovoltaics (EPV)

IEC has continued collaboration with EPV on alternative back contacts. A paper partly on this work was presented at the 2005 AVS International Symposium in Boston "TiN and TiO2:Nb thin film preparation using hollow cathode sputtering with application to solar cells" by S.Y. Guo, W.N. Shafarman, and A.E. Delahoy.

Purdue University

IEC has reacted novel precursor films in H_2Se to help Purdue's effort to develop alternative processes for Cu(InGa)Se2 formation.

University of Nevada, Las Vegas

IEC has begun collaboration with Clemens Heske at UNLV in a project to study the absorber/back contact interface in terms of its chemical and electronic properties. Specifically, IEC provided 5 samples, including glass/Mo/Cu(InGa)Se_2 and glass/Mo/Cu(InGa)$(SeS)_2$. A procedure for packaging the samples with minimum air exposure was developed for shipping these samples. Initial studies will include photoemission and inverse photoemission measurements on the front surface and on both surfaces of the Mo/Cu(InGa)Se_2 interface after peeling the film from the substrate.

University of Oregon

IEC and Oregon continue to collaborate closely to characterize opto-electronic properties of solar cells with Cu(InGa)Se_2 as a function of absorber alloy composition, sodium incorporation, and other processing conditions, with IEC providing sample sets with different compositions or substrates for analysis.

University of Syracuse

IEC has begun collaboration with Eric Schiff at Syracuse to characterize electronic transport properties of Cu(InGa)Se_2. A set of 3 Cu(InGa)Se_2 device samples was sent and will be characterized by drift-mobility measurements.

University of Toledo

IEC provided Cu(InGa)Se_2 device samples for piezoelectric measurements.

3.6 Phase 6 Summary: 4/1/07 to 12/31/07

In the subtask "In-Line Evaporation of $Cu(InGa)Se_2$" the research objective was to determine the limit of deposition time for $Cu(InGa)Se_2$ in-line evaporation in IEC's roll-to-roll process and the effects of higher speed deposition on device performance. Our approach was to deposit $Cu(InGa)Se_2$ with increasing web translation speed and source effusion rate and characterize the resulting device performance as a function of thickness and growth rate.

A second sub-task focused on "Improved Performance with Absorber Thickness < 1 μm." In this area the objective was to develop methods to increase J_{SC} in devices using absorber layers with thickness $0.3 \leq d \leq 1.0$ μm. The approach was to develop methods to implement light scattering into $Cu(InGa)Se_2$ devices and determine its potential for increasing J_{SC}. Determine if the higher absorption coefficient in $CuInS_2$ or S-containing alloys can be used to increase J_{SC} with thin absorbers.

To further characterize films and devices with submicron $Cu(InGa)Se_2$ thicknesses, films were evaporated using constant deposition rates and varying times to form layers with thicknesses from 0.35 – 3.3 μm. Characterization of the films showed that the grain size decreases significantly as thickness is reduced less than 1 μm. Devices showed a decrease in performance with decreasing thickness attributed primarily to reduced J_{SC}. A device with $Cu(InGa)Se_2$ thickness 0.35 μm had $V_{OC} > 0.6$ V and FF > 70% but efficiency 7.9% due to the loss in J_{SC}.

Thin $CuInS_2$ absorber layers were deposited and compared to results with $Cu(InGa)Se_2$ to determine the effect of the higher absorption coefficient in the S alloy. The films had a similar reduction in grain size with decreasing thickness. The $CuInS_2$ devices had a loss in J_{SC} which was greater than expected from the optical absorption but the relative decreases in J_{SC} and long wavelength QE were less than with comparable thickness $Cu(InGa)Se_2$. To implement light scattering into $Cu(InGa)Se_2$ devices experiments were done to determine if ITO films could be sufficiently textured using a post-deposition etch. It was found that the films could be textured with HCl but efforts to implement this into processing of $Cu(InGa)Se_2$ cells was not successful with either shunting or very low current.

A third subtask on $CuInSe_2$-based solar cells has focused on "Increased V_{OC} for Improved Module Performance." In this effort our objective was to develop processes to increase V_{OC} in $Cu(InGa)(SeS)_2$ solar cells by controlling film growth and composition. This work has focused on controlling the composition of the pentenary $Cu(InGa)(SeS)_2$ in its formation by the reaction of Cu-Ga-In precursors in H_2Se and H_2S and in elemental co-evaporation to deposit $Cu(InGa)(SeS)_2$.

For $Cu(InGa)(SeS)_2$ films formed by 5-source elemental evaporation we have previously determined the effect of changes in [Cu]/[In+Ga] and [Ga]/[In+Ga] on the relative S incorporation at 550°C substrate temperature. In this work, the dependence of the relative Se and S incorporation chalcogen in $Cu(InGa)(SeS)_2$ on the substrate temperature

was characterized with various [S]/[Se+S] flux rate ratios of at T_{SS}. The chalcogen incorporation is the same at 450 – 550°C for both Cu-excess and Cu-deficient growth. However, at 300°C the relative [S]/[Se+S] composition changes when films are grown without excess Cu. The chalcogen incorporation is compared to predictions from equilibrium thermodynamics and to an empirical kinetic model.
For $Cu(InGa)(SeS)_2$ films formed by the reaction of $Cu_{0.8}Ga_{0.2}$/In precursors, a sequential H_2Se/H_2S reaction process has been used to control through-film composition, avoiding the accumulation of Ga at the back of the film which occurs with reaction in only H_2Se. The effect of reaction temperature on film formation and compositional uniformity was evaluated in precursors first selenized in H_2Se at 450ºC for 15 minutes, then sulfized in H_2S for 30 minutes at fixed temperatures over the range 450 to 550ºC. An abrupt increase in the degree of Ga homogenization is observed for samples sulfized at temperatures of ~500ºC and above, along with a more general increase in S incorporation in the film with increasing temperature.

Finally, methods are being investigated to control through-film composition in the formation of $Cu(InGa)(SeS)_2$ films by the reaction of metal precursors by incorporating a copper selenide layer in the precursor to circumvent the formation of Cu-Ga-In intermetallic phases. CuSe/Ga/In and $Cu_{2-x}Se$/Ga/In precursors were formed by combinations of electrodeposition, annealing, and electron beam evaporation of Ga and In and compared to the sputtered $Cu_{0.8}Ga_{0.2}$/In precursors. The relative Ga distribution through the film was characterized by XRD and EDS measurements and shown to vary with the different precursor structures. Device results suggest that the precursors containing the binary Cu-selenide phases are reacted in less time than the metallic precursors.

CIGS TFP Team Activity and Collaboration

IEC has collaborated with, or provided assistance to, several other university of industrial groups working on $Cu(InGa)Se_2$ solar cells in the past year. These include:

<u>Ascent Solar, Dow Chemical, HelioVolt, Nanosolar, SoloPower, Solyndra</u>

IEC has leveraged its expertise, baseline processes, and characterization facilities to assist these $Cu(InGa)Se_2$ companies in a variety of ways, including:

- reacting precursor films to form $Cu(InGa)(SeS)_2$ and characterizing the resulting materials.
- fabricating cells to validate their cell fabrication processes.
- analysis of materials and devices supplied by the companies.
- supplying films or devices for comparison to their materials or calibration of their measurements.

<u>Battelle – Pacific Northwest National Laboratory</u>

Baseline IEC $Cu(InGa)Se_2$ devices were provided to Larry Olsen for encapsulation and stability studies including damp heat tests.

University of Florida

IEC prepared samples for studies of reaction chemistry and kinetics to the group of Tim Anderson. Specifically, stacked (Ga-Se)/(Cu-Se) samples along with control samples from the separate Ga-Se and Cu-Se runs were deposited.

University of Illinois

IEC provided $Cu(InGa)Se_2$ films to the group of Angus Rockett for photoluminescence measurements. These included different films with varying [Cu]/[In+Ga] and [Ga]/[In+Ga] composition ratios.

University of Nevada, Las Vegas

$Cu(InGa)Se_2$ and $Cu(InGa)(SeS)_2$ films were sent to the UNVL group of Clemens Heske for IPES/UPES measurements to characterize the electronic structure of the films. These include a wide range of different compositions including systematic variation in [Cu]/[In+Ga], [Ga]/[In+Ga], and [S]/[Se+S].

University of Oregon

IEC and Oregon continue to collaborate closely to characterize opto-electronic properties of solar cells with $Cu(InGa)Se_2$ as a function of absorber alloy composition, sodium incorporation, and other processing conditions, with IEC providing sample sets with different compositions or substrates for analysis. In this contract period IEC prepared and sent two sets of samples. The first was a set of $Cu(InGa)(SeS)_2$ devices with fixed $[S]/[Se+S] \approx 0.25$ and varying [Ga]/[In+Ga] and the second was a set of devices with soda lime glass and Ti foil substrates to control the Na content.

3.7 Phase 7 Summary: 1/1/08 to 5/31/08

Composition Control for Increased V_{OC}

In this task we are investigating processes to increase V_{OC} in $Cu(InGa)(SeS)_2$ solar cells using absorber layers formed by the reaction of precursors in H_2Se / H_2S which is typically low due to accumulation of Ga at the back of the reacted film. A two-step reaction of Cu-Ga-In precursors with partial reaction in H_2Se at 400° – 450°C followed by completion in H_2S at 550°C has been used to form $Cu(InGa)(SeS)_2$ films with uniform incorporation of the Ga.[1] To provide a basis for improvements in device performance, efforts are being undertaken to improve the IEC H_2Se/H_2S baseline process to improve reproducibility. Current studies into the effect of sulfization temperature on Ga homogenization have yielded several possible approaches to improve process reproducibility.

$Cu_{0.8}Ga_{0.2}$/In precursor bi-layers were selenized at 450ºC for 15 minutes, followed by sulfization at temperatures ranging from 450° – 550ºC for 30 minutes. Two samples

were processed side-by-side for each run in an "upstream" and "downstream" orientation. Samples were characterized by SEM/EDS, XRD, and AES depth profiling.

Figure 1 shows Ga/(Ga+In) ratios measured by EDS for sulfization temperatures over the range 450° – 550ºC. Since EDS is sensitive to the top 0.5 – 1 μm of the 2 μm film, it is useful for characterizing the degree of Ga homogenization in a sample. If the Ga/(Ga+In) ratio measured by EDS is equivalent to the known ratio based on precursor sputter thicknesses, it can be reasonably concluded that a uniform Ga profile exists in the sample. Figure 1 shows that a sulfization temperature of ~500ºC is necessary, but not sufficient, to achieve a uniform Ga profile.

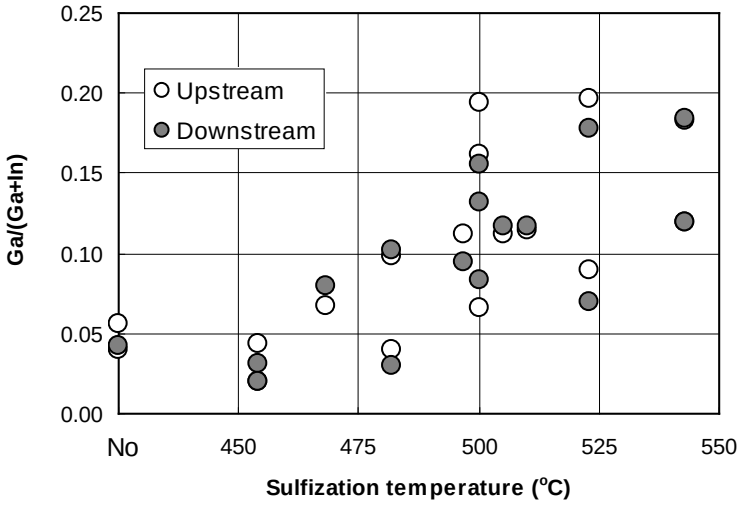


Figure 1. Ga/(Ga+In) ratio in H_2Se/H_2S-reacted precursor films measured by EDS over a range of sulfization temperatures.

Figure 2 shows (112) d-spacings of the same samples, and indicates an abrupt decrease in d-spacing, indicating a higher degree of either Ga or S incorporation into the chalcopyrite lattice, at temperatures of 500ºC and above. As with the EDS data, there is a wide range of d-spacings observed at temperatures above 500ºC. However, there is an additional result of interest in that upstream and downstream samples processed side-by-side at temperatures between 500° – 510ºC repeatedly exhibit d-spacings on either side of the apparent "gap" between ~3.318 Å and ~3.301 Å. This suggests a high sensitivity to process conditions in this temperature range.

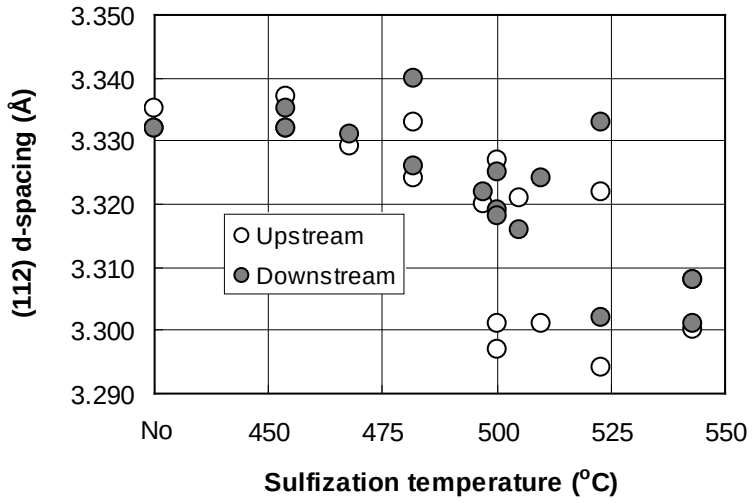


Figure 2. Chalcopyrite (112) d-spacing for H_2Se/H_2S-reacted samples over a range of sulfization temperatures.

The samples in Figure 1 exhibiting Ga/(Ga+In) < 0.12 at sulfization temperatures exceeding 520ºC, and the samples in Figure 2 exhibiting d > 3.320 in the same temperature range suggest that there are variables in the existing baseline H_2Se/H_2S process that are not fully understood. It is already known that the degree of selenization influences the degree of Ga homogenization that occurs during sulfization.[1,2] It is further known that thermal characteristic times in the existing chalcogenization system are on the order of minutes.[3] Therefore, the samples are heating up for a substantial fraction of the 15-minute reaction time. It is therefore suggested that the baseline H_2Se/H_2S process be modified to utilize a reduced selenization temperature. This will slow down the reaction rate, allowing longer selenization times of which thermal transients represent a much smaller fraction of the reaction time. It is expected that this will result in more reproducible degrees of selenization.

Based on the high degree of (112) d-spacing sensitivity during sulfization at temperatures in the range 500° – 510ºC, it is contemplated that the Ga homogenization and sulfization mechanisms may be in competition with one another. It can be inferred that Ga is substantially immobile once is has been incorporated in the chalcopyrite lattice – this is based on the reduced Ga homogenization as degree of selenization increases. As sulfur reacts with Ga-bearing intermetallics, it is driving its incorporation into the chalcopyrite lattice, reducing its mobility. Thus, the homogenization of Ga may be dependent on both temperature and S concentration. A second suggestion for improving the baseline H_2Se/H_2S process is to incorporate an inert anneal at temperatures between 500° – 550ºC before the introduction of sulfur. This also suggests the possibility of reduced Ga homogenization with increased H_2S concentration. This approach has the further benefit making a fundamental determination of whether temperature or sulfur is the driving force for Ga homogenization. It should be noted that Marudachalam found that Ga could be homogenized in fully selenized films by an inert anneal at temperatures above 500ºC.[4]

A second approach to increase V_{OC} using films formed by the reaction of precursors is to control the relative through-film Ga composition by circumventing the formation of Cu-Ga-In intermetallic phases using mixed metal/metal-selenide precursors. Formation of a relatively stable Cu_9Ga_4 phase was identified as a cause of the Ga segregation to the back of the film.[5]

In a previous report, copper selenide was prepared by electrochemical deposition onto Mo-coated soda-lime glass substrates and annealing to form either $Cu_{2-x}Se$ or CuSe phases. Reaction in H_2Se gave $Cu(InGa)Se_2$ films that maintained a through-film Ga gradient even though no intermetallic phases were detected by XRD after short reaction times. In this report we show results with two additional precursor combinations. The first was formed by co-evaporation of Cu and Se with a substrate temperature of 520ºC followed by Ga and In layers deposited by electron-beam evaporation. The second was a $(In,Ga)_2Se_3$/Cu precursor formed with Ga and In layers sequentially deposited onto the substrate by e-beam evaporation and selenized for 60 minutes at 350ºC at atmospheric pressure followed by an e-beam evaporated Cu layer. As a control, $Cu_{0.8}Ga_{0.2}$/In precursors with a composition of Cu/(In+Ga) = 0.9 and Ga/(In+Ga) = 0.2 were prepared by sequential sputtering. All precursor types had Cu/(In+Ga) = 0.9 and Ga/(In+Ga) = 0.2 with thicknesses determined to yield 2 µm $Cu(InGa)Se_2$ films. The precursors were selenized for 5, 15 or 90 min (only 15 or 90 min for the $(In,Ga)_2Se_3$/Cu precursor) at 450ºC at atmospheric pressure in a quartz tube reactor using a 0.35at% H_2Se/0.0035at% O_2/Ar gas mixture.

XRD measurements were used to confirm the selenide phases in the as-deposited precursors and after the H_2Se reactions. The latter results are listed in Table I. With the precursors containing the selenide phases there were no intermetallic phases observed, unlike with the $Cu_{0.8}Ga_{0.2}$/Ga control.

Table I. Phases identified by XRD with different precursors.

Precursor structure	reaction time (min)	Identified phases
$Cu_{2-x}Se$/Ga/In	5	$Cu_{2-x}Se$, InSe, In_6Se_7
	15	$Cu(InGa)Se_2$
	90	$Cu(InGa)Se_2$
$Cu_{2-x}Se$/Ga/In	5	N/A
	15	InSe, GaSe, $Cu(InGa)Se_2$
	90	$Cu(InGa)Se_2$, $MoSe_2$
$Cu_{0.8}Ga_{0.2}$/In (control)	5	InSe, $Cu(InGa)Se_2$, Cu_3Ga, $\gamma 1$-$Cu_9(In,Ga)_4$
	15	$Cu(InGa)Se_2$, $\gamma 1$-$Cu_9(In,Ga)_4$
	90	$Cu(InGa)Se_2$, $MoSe_2$

Compositions were determined measured by EDS from the top and backside of the films using a film lift-off technique for the latter measurements. The [Ga]/[In+Ga] ratios after different selenization times are shown in Figures 3 and 4 for the two different mixed

metal/metal-selenide precursors. Both cases showed Ga accumulation at the back of the $Cu(InGa)Se_2$ film, although the Ga gradient may be smaller with the $(In,Ga)_2Se_3$/Cu precursor.

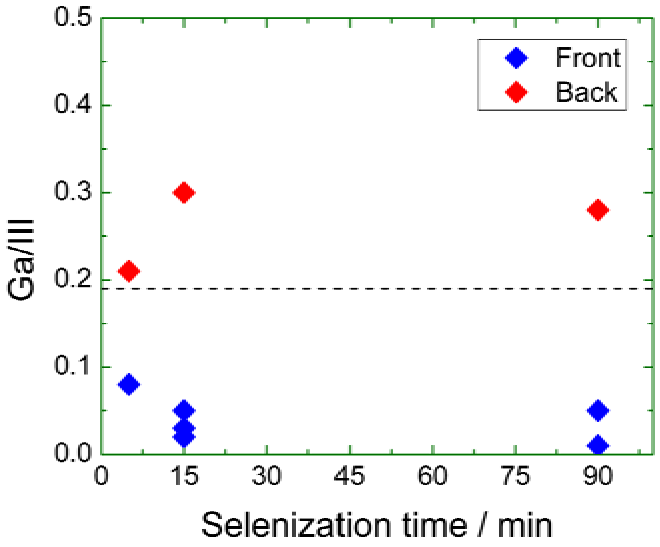


Figure 3. [Ga]/[In+Ga] ratios measured by EDS from the top and back sides of $Cu_{2-x}Se$/Ga/In precursor films selenized for different times. The dashed line shows [Ga]/[In+Ga] in precursor.

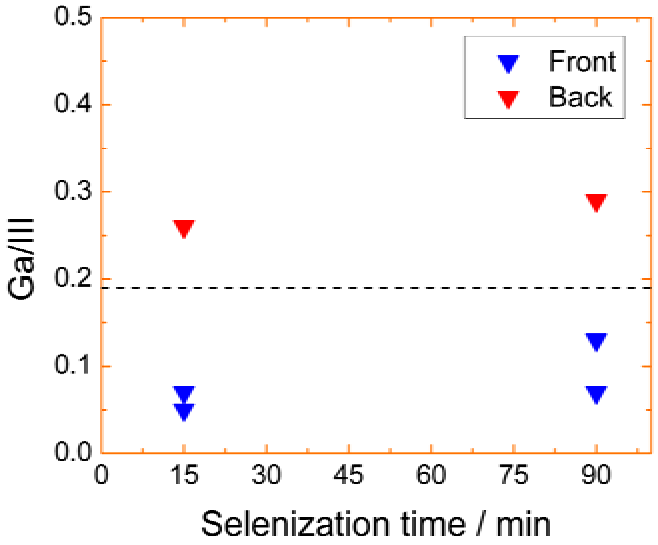


Figure 4. [Ga]/[In+Ga] ratios measured by EDS from the top and back sides of $(In,Ga)_2Se_3$/Cu precursor films selenized for different times. The dashed line shows [Ga]/[In+Ga] in precursor.

Device results of the solar cells made from the precursors following 90 min selenization reactions are shown in Table II. No increase in V_{OC} was obtained with either of the mixed metal/metal-selenide precursors compared to the sputtered metal precursor.

Table II. Device J-V parameters of the solar cells made from the selenized precursors.

Precursor	V_{OC} (V)	J_{SC} (mA/cm^2)	FF (%)	η (%)
$Cu_{2-x}Se$/Ga/In	0.439	37.2	62.4	10.2
$(In,Ga)_2Se_3$/Cu	0.332	32.9	38.1	4.2
control	0.474	36.8	50.5	8.8

In-Line Evaporation

Na Incorporation:

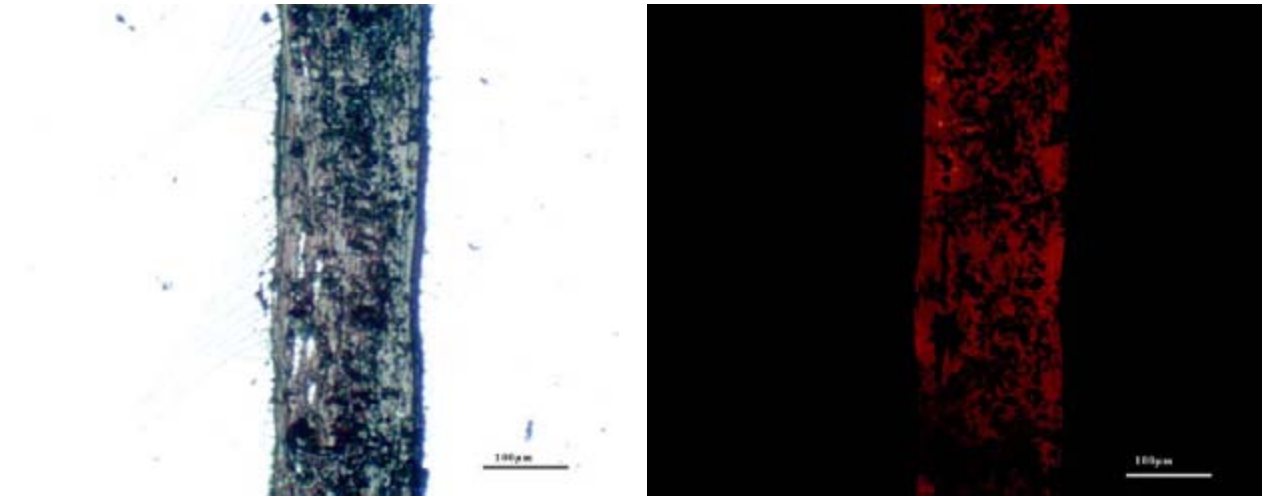
A NaF effusion source identical to other sources in the system was placed such that it would be 1st source in the direction of travel during the 2nd pass. The shield that forms the deposition zone partially covers effusion from the Na source. The initial Na source temperature was chosen to give an approximate effusion rate of 0.1% that of Cu. Since the sources are geometrically identical this temperature would correspond to NaF vapor pressure equal to 10^{-3} of the vapor pressure of Cu for the standard operating condition. For the Cu source temperature operating at 1400°C this gives a NaF source temperature of 685°C.

Two sets of experiments were performed at the Na source temperature of 685°C. Initially, NaF was turned on during the 1st pass where it was the last source seen by the substrate carrier traveling at 18"/min. Devices made on Upilex substrates did not show any improvements in V_{OC} or FF relative to our baseline. This could be the consequence of high speed substrate travel and low source temperature both of which tend to reduce NaF deposited on the substrate. As a result, a second set of runs were performed keeping the NaF source at the same temperature but moving the evaporation to the 2nd pass when substrate NaF is the 1st source and substrate travel is only 2"/min. Even under these conditions no effect was observed on the devices fabricated on Upilex substrates. The next set of experiments will follow the same protocol except for the NaF temperature which will be increased to give a vapor pressure of $5x10^{-3}$ that of Cu.

Monolithically Integrated Flexible Modules:

Scribing tests for monolithic integration by mechanical and laser scribing have been started. Initial attempts in mechanically scribing the molybdenum (Mo) layer (P1 scribe) with a programmable x-y mechanical scribing system resulted in tearing of the Upilex. Double stick tape was then used to secure the Upilex giving much improved results. However, the resulting scribe showed only partial removal of the Mo layer as can be seen in Figure 5 where the optical microscopy image of the mechanical scribe is shown both in reflection and in transmission. Note that even though the back side of the Upilex substrate is coated with 20 nm of Mo it does let enough light go through to have adequate observation in transmission.

In the case of scribing the $Cu(InGa)Se_2$ layer (P2 scribe) it was found that even the lightest pressure between the scribe tip and the sample would always remove the Mo from the Upilex. This was in contrast to the films on glass substrates where the P2 scribe left Mo film intact. As a result, the decision was made to test laser scribing for both P1 and P2 scribes.



A B

Figure 5. Optical microscope image of mechanically scribed Mo on Upilex viewed in reflection (A) and transmission (B).

Initial tests were made with the laser parameters that were successfully used for glass substrates. Figure 6 is the optical micrograph of the P1 scribe performed with the 532 nm laser. In this case, the Mo films were removed completely but there is substantial thermal modification to the Upilex at the center of the scribe.

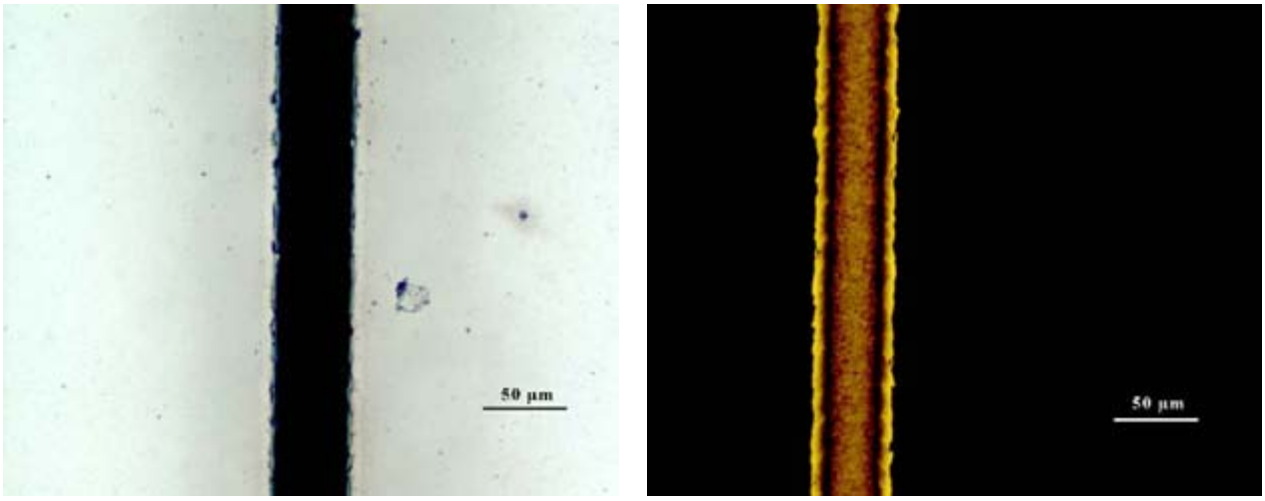


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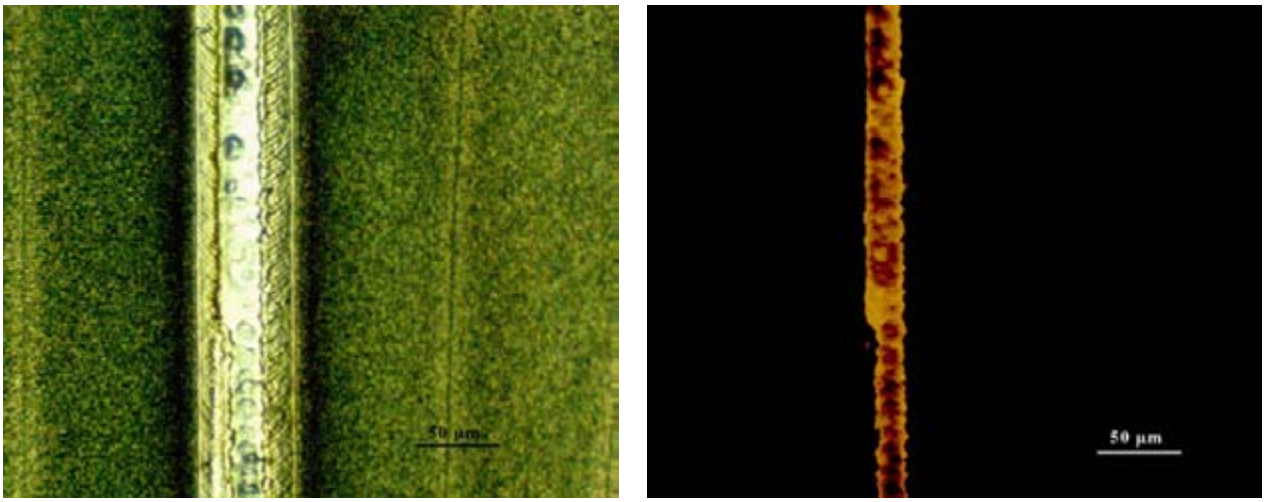
Figure 6. Optical microscope image of laser scribed Mo on Upilex viewed in reflection (A) and transmission (B).

The P2 scribe on the films on Upilex is shown in Figure 7. The scribe was again made using the 532 nm laser based on the experience from the glass substrates. The micrographs are clear showing that the cut not only removes $Cu(InGa)Se_2$ but also the Mo layer and part of the Upilex substrate. From these tests it is clearly evident that much less aggressive laser scribing needs to be investigated.



A B

Figure 7. Optical microscope image of laser scribed $Cu(InGa)Se_2$ on Mo coated Upilex viewed in reflection (A) and transmission (B).

3.8 References

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4 Si- BASED SOLAR CELLS

4.1 Phase 1 Summary: 9/5/01 to 9/4/02

During the first year of the program, an in-situ grain enhancement process involving HWCVD Si films deposited on Al-coated glass substrates was evaluated. Two substrate temperatures, 400 and 600 ^{0}C, were investigated so as to study conditions below and above the Si-Al eutectic temperature (575 ^{0}C). For films deposited at 600 ^{0}C, delamination and non-uniform properties were observed. It is believed this was caused by poor wetting characteristics at the Al-glass interface which led to non-uniform Al coverage on the glass substrates. For films deposited at 400 ^{0}C, the Si film grain structure, average grain size and crystalline fraction were compared as a function of the growth rate, Si/Al ratio and Si film thickness. In general, the Si film crystalline fraction and average grain size increases with decreasing growth rate, Si/Al ratio and Si film thickness. A maximum average grain size of 100 nm as measured by XRD peak broadening was achieved at 1.0 μm/hr growth rate in a 2.0 μm thick Si sample with a Si/Al ratio of 2. This sample also exhibited a Raman peak profile closely resembling that of bulk c-Si. Further characterization by TEM revealed that the film had a bimodal grain size distribution with regions of nanometer and micron-sized grains. For 5 μm thick Si films, regardless of the growth rates and Si/Al ratios considered, the Si film average grain size and crystalline fraction were 10-50 nm and 75-80%, respectively. This suggests that the growth of micron size crystallites does not continue as the thickness of Si film increases beyond a critical value. At a growth rate of 5 μm/hr, films are similar to those grown on glass with average grain size less than 50 nm and crystalline fraction of ~75%.

A series of p-i-n and n-i-p devices were fabricated in order to evaluate the opto-electronic properties of the HWCVD polycrystalline Si i-layers. The devices were fabricated on both n-type and p-type c-Si wafers with the window layers consisting of PECVD n- and p-μc-Si, respectively. Two i-layer thickness values were considered, 2 and 10 μm. In general, all devices showed little rectification in light or dark. The n-i-p's had J_{sc} ~2 mA/cm^2 and V_{oc} ~30 mV while p-i-n's showed no photovoltaic behavior. The results from these devices and accompanying n-i-p and p-i-p diagnostic devices lead to the conclusion that the i-layer is highly defective and has significantly short diffusion lengths for both holes and electrons. Devices were also fabricated on small grain μc-Si HWCVD i-layers grown on Al-glass substrates. The structure was glass/μc-Si-Al (HWCVD)/μc-Si i-layer (HWCVD)/μc-Si n-layer (PECVD)/ZnO/grids. The devices were typically shorted. Subsequent analysis has found Al metal penetration to the top of the HWCVD film which could be responsible for the shorting behavior.

A study of optical losses and enhancement in a-Si devices on textured SnO_2 substrates was undertaken using PVOPTICS, a modeling program developed at NREL by Dr. Bhushan Sopori. Comparison of simulation results with measured photocurrent data obtained from integrating the spectral response at reverse bias with the AM1.5 spectrum in the range of 400-800 nm shows good agreement for a range of devices varying in thickness, texture and back contact reflectivity. The simulations indicated that while the

use of textured SnO_2 and Al back reflector increase the photocurrent, these gains are partially nullified by equivalent absorption losses in the red region at the front and back contacts. Parasitic losses at the front and back contact occurred for texture angles greater than 10°. Increasing the angle causes better internal trapping in the i-layer, but also higher SnO_2/a-Si reflection losses, as well as SnO_2 and metal absorption losses. Parasitic absorption in the textured SnO_2 due to back reflected light is 1-2 mA/cm^2 for typical designs. N-i-p cells have a fundamental advantage over p-i-n cells since the textured TCO is at the rear of the device leading to lower losses. Light trapping in even simplified device structures with textured interfaces can be very complex. The angle of texture can have competing influences which can lead to increases or decreases in J_{PH} depending on other design parameters. Increasing the angle of the texture results in less reflection losses and better light trapping, hence higher photocurrents, but also larger parasitic absorption losses in the SnO_2 and metal BR.

The original PVOPTICS program had no data files for the optical constants n and k to model SnO_2 films. We measured several commercial SnO_2 films using our VASE and provided the results to Sopori who incorporated them into a special version of PVOPTICS for IEC use in the above analysis. However, we have been concerned about characterization of VASE on textured surfaces such as SnO_2. We carried out VASE measurements on mechanically polished and unpolished Asahi Type U textured SnO_2. Polishing significantly reduced but did not eliminate texture. We developed the optical model for the polished film first and then import the textured SnO_2 film data in to this optical model. We used a two-layer structure with surface roughness modeled using an effective medium approximation (EMA) layer. For polished films the fit looks excellent. However, for the textured film the fit is not very good, at the higher energy region where the roughness plays a significant role.

The depolarization is a strong function of texturing not sample nonuniformity as reported by others. We suspect that this difference is due to the difference in incident angle used between different groups. Our results indicate that the depolarization is caused by the textured surface.

Thin Si TFP Team Activity and Collaboration

IEC continued providing leadership in the Multijunction Device Team. A presentation was made summarizing the literature on TCO/p contact properties followed by a application of a new method developed at IEC to characterize this contact. It was applied to devices made at IEC on SnO_2 and ZnO (from Harvard Univ) and at BP Solar using various interfaces on SnO2 and SnO_2/ZnO bilayers. The method was applied to laser scribed minimodules. A key result was that there is no blocking contact or very high resistance between ZnO and p-layers, as is commonly assumed. Instead the diode recombination increased, leading to reduction in Voc and FF.

4.2 Phase 2 Summary: 9/5/02 to 9/4/03

The grain size enhancement of HWCVD Si films deposited on Al layers has been investigated in two temperature regimes. These regimes are determined by the eutectic temperature of 575°C in the Si-Al system. With the formation of a liquid phase above the eutectic temperature, a different mechanism is expected to govern the grain enhancement process compared to that expected below this temperature where the Si-Al mixture remains in the solid state. This report describes the results obtained for depositions of HWCVD Si films on Al layers at 430°C and 600°C.

Aluminum layers with thickness varying from 0.01 to 1.0 μm were deposited onto Corning 7059 type glass substrates using electron-beam evaporation. Silicon layers were subsequently deposited onto the Al coated samples in the HWCVD system. Silane was used as the source gas with no hydrogen dilution. Silicon layer depositions were carried out at a substrate temperature of 430°C and 600°C, filament temperature of 1850°C and pressure of 25 mTorr. The films were deposited at two different growth rates of 1.0 and 5.0 μm/hr, which were attained by varying the silane flow rate from 4.5 to 22.5 sccm, respectively. Films with thickness values of 2 and 5 μm were deposited with deposition times corresponding to 24 min and 5 hrs, respectively.

For deposition at 430°C, Raman spectroscopy and XRD showed Si films deposited on Al had random orientation and higher degree of crystallization compared to films deposited on glass. The crystalline Si Raman profile of films deposited on glass had a typical tail extending toward lower wavenumbers indicative of a-Si and nanocrystalline Si phases. In contrast, films deposited on Al, had profiles similar to those obtained for c-Si. For 2 μm thick films grown at 1 μm/hr, the average grain size and crystalline fraction increases with decreasing Si/Al ratio. The maximum average grain size of 200 nm was achieved with a Si/Al ratio of 2. As the growth rate is increased from 1 to 5 μm/hr, the average grain size and crystalline fraction decreases at a constant Si/Al ratio. AFM analysis revealed that some areas on the film surface are covered with small particles, 10-50 nm in diameter. It is speculated that these features are individual grains, which do not extend throughout the bulk of the Si film. TEM analysis found heterogeneous structure of several large grains but mostly nano-crystalline regions. These two crystalline regions can be found either side by side on the Al layer or as layers with one evolving from the other. It is speculated that the presence of the nano-crystalline phase indicates an incomplete grain enhancement process and that the effect of lower growth rate for given film thickness is to increase the interaction time between the layers. The poly-Si does not form a continuous layer. The bulk of the films also contain Al. Al layer inversion is incomplete, perhaps due to insufficient interaction time between the Si and the Al layer. For 5.0 μm thick samples the average grain size varied between 40 and 70 nm, and the crystalline fraction did not change significantly with the growth rate. The decrease in grain size for Si films with 5 μm thickness may be due to the existence of a limiting thickness beyond which the Al ceases to have an effect on the growth process. If this hypothesis is correct, the film evolves from a large grain to a nanocrystalline grain microstructure as seen on films deposited on glass.

Si films deposited at 600°C exhibit larger average grain size as measured by XRD peak broadening. This contrast is more pronounced as the growth rate and Si film thickness increases. However, all films were non-homogeneous in terms of morphology and composition perhaps as a result of poor wetting of the Al layer on the 7059 glass at 600°C or alternatively due to segregation of the liquid phase forming at the eutectic composition. On average, the crystalline volume fraction of films deposited at 600°C is similar to those deposited at 430°C.

Fabrication of p-i-n solar cells with all PECVD µc-Si layers was investigated on glass/SnO_2 substrates. The 2.0 µm i-layer was deposited for 9 hours. No ZnO or a-Si buffer layers or any other transitional layers were incorporated. Device performance was very poor, with V_{OC}=0.2V and efficiency <1%. CV and QE measurements suggested a relatively high defect density and low barrier height. The µc-Si devices have substantially more absorption below the a-Si absorption edge confirming that their structure is between a-Si and c-Si.

Thin film Si n-i-p solar cells were fabricated on n-doped c-Si substrates using PECVD and HWCVD microcrystalline i-layers. No metal induced crystallization was utilized. The structure of the devices was Ag-Pd-Ti/n^+-cSi/(PECVD or HWCVD) i-µcSi/PECVD p-µcSi/ITO/Ni-Al. The n+ wafer substrates served as the n-layer in the p-i-n cells. In addition, diagnostic n-p devices were fabricated by depositing PECVD p-µcSi emitter layers directly onto the n^+-c-Si substrates. Identical n-i-p and n-p devices were also fabricated which incorporated a 30 nm a-Si buffer layer between the p-layer and i-layer or n+ c-Si. The performance of all solar cell devices was quite poor. All cells with a HW or GD i-layer absorber had less than 1% efficiency although many had well formed diode characteristics in light and dark.

Both n-i-p and n+/p+ cells using GD and HW µc-Si absorber i-layers have produced cells with poor photo-carrier collection and high recombination. The a-Si buffer layer increases V_{OC} but reduces J_{SC} and FF in both n-i -p and n+/p+ cells. No first-order differences were seen between devices the HW or GD µc-Si layers. n+/p+ cells with the a-Si buffer achieved V_{OC}=0.62 V but with very poor J_{SC} and FF.

Previously, standard a-Si p-i-n devices routinely achieved FF=70% while recently FF has been limited to 50-60%. QE measurements indicated poorhole collection from the i-layer. The most likely cause is donor-like impurities such as P or O, which reduce the lifetime of the hole. Considerable effort was made in cleaning or modifying the PECVD deposition system to eliminate possible sources of O or P. None of these changes resulted in a higher FF. Select samples were sent to NREL for SIMS analysis. Since our PECVD reactor is a single chamber system, a major concern in both a-Si and µc-Si devices is the P and B cross-contamination. Results showed that P and B are quite low in PECVD and HWCVD a-Si films and devices. Some recent devices have had B concentrations of 10^{18} cm^{-3} in the p-layer while P was 10 times higher. This suggests our burying layer is not effective anymore in preventing P cross-contamination. Consequently, a new burying procedure is being implemented. For PECVD or HWCVD

μc-Si devices, the concentration of O, N and C are several orders of magnitude higher than those in the a-Si cell and the c-Si wafer, as is reported by others. These impurities in the HWCVD samples have a concentration gradient, which decreases from the top surface and level off to a constant bulk concentration at approximately one micron into the film. It is speculated that the lower H content in HWCVD films combined with the excessive number of grain boundaries and film porosity may facilitate contaminant penetration into the films.

Boron doped HWCVD films were deposited and characterized. Films were polycrystalline with typical (220) preferred orientation. Crystalline fraction was 75 to 90%. A dependence of conductivity with dopant gas concentration and film thickness was found. For submicron films, conductivies were constant at 10^{-6} S/cm for B_2H_6/SiH_4 $<10^{-3}$. At $B_2H_6/SiH_4 = 10^{-2}$, the conductivity reached 10^{-3} S/cm. For films with thickness > 2 μm and $B_2H_6/SiH_4 = 10^{-2}$, the conductivity further increased to 10^{-1} S/cm. The effect of thickness on conductivity points to a change in microstructure as the film thickness increases. This hypothesis is corroborated by activation energy data, which indicates a change in mobility with thickness. Future work will include a determination of the effects of film microstructure and dopant gas concentration on film conductivity.

Thin Si TFP Team Activity and Collaboration

IEC attended the National Thin Film Si Team Meeting held on January 10. 2003 and gave a presentation on the growth and characterization of HWCVD Si films on Al coated glass. We also attended the National Thin Film Si Team Meeting on August 8, 2003 and gave a presentation on the grain enhancement of Si films by aluminum induced crystallization approaches.

IEC received 9 plates of a-Si devices from Dr. Gautam Ganguly at BP Solar for measurements and analysis to determine the contact resistance and diode A factor. One series compared textured AFG SnO_2 and Harvard ZnO with and without buffer layer deposition before the p-layer. The other series compared different back contact buffer layers. We analyzed the devices as described previously using dark JV measurements on a row of 6 devices per plate to determine the contact resistance, TCO sheet resistance, and diode properties. We found that certain buffer layers significantly decreased the contact resistance. Consistent with results in the above paper, we found that direct deposition onto ZnO leads to much higher A factor ~ 3, not higher contact resistance. The buffer layer allows A to remain ~1.6 as typical of good devices with low contact resistance. This work was subsequently published (Ganguly, Hegedus et al, Appl Physics Lett 85, 2004, 479-481).

4.3 Phase 3 Summary: 9/5/03 to 9/4/04

Post-deposition annealing experiments of Al/Si bi-layers were carried out to compare crystallization and layer inversion processes in standard metal induced crystallization and in-situ metal induced crystallization. Evaporated Si films allowed comparison between films deposited in an H free environment and HWCVD films. First, 0.5 mm thick films

of Al were deposited onto 7059 glass substrates by electron beam evaporation. The films were left in ambient air for a period of 24 hr to allow formation of an oxide layer. Si films with 0.6 mm thickness were then deposited by electron beam evaporation and HWCVD. XRD measurements showed no evidence of crystallization of the Si films deposited by evaporation prior to annealing while films deposited by HWCVD were completely crystallized. Annealing was performed for 90 min at 500°C under 100 sccm of Ar. For Si films deposited by evaporation, optical microscopy showed polycrystalline Si nucleation extending to the glass interface with very little lateral grain growth. XRD analysis showed only partial crystallization of these films. For samples with Si films deposited by HWCVD, no increase in grain coalescence or crystalline fraction was observed.

Work continued on in-situ crystallization during HWCVD growth. Analysis of HWCVD Si films deposited on Al coated glass substrates below the Si-Al eutectic temperature (~570°C) revealed a layered microstructure. The lower layer near the glass interface is composed of micron size islands of polycrystalline silicon. Atop this layer, a mixture of nanocrystalline Si and Al remains. This mixture is also observed in the spaces between the polycrystalline Si islands. The existence of this layered structure is evidence of layer inversion and is consistent with standard metal induced crystallization results obtained by other groups. However, the discontinuity of the underlying polycrystalline Si structure limits its usefulness for device fabrication. Raman spectroscopy through the glass substrate confirms regions of polycrystalline Si and regions of a mixture of nanocrystalline Si and Al. After etching the overlaying Si-Al mixture, a similar pattern of polycrystalline Si islands is observed from the front surface. Post-deposition anneal at 430 °C under vacuum for 2 hours increased the fractional coverage of c-Si from 60 to 90%. This indicates that the excess Si does not crystallize as it accumulates on the Al layer surface during deposition and is available for further lateral growth of the polycrystalline Si layer.

The average grain size appears to decrease with increasing Si/Al ratio and correlates well with the time the Al layers remained exposed to air prior to Si film deposition. The role of aluminum oxides on the layer inversion process and grain size of the polycrystalline Si layer is not well understood. It is hypothesized that the oxide layer acts as a nucleation barrier leading to a lower density of near neighbor nuclei. However, it is expected that the oxide layer is self-limiting and would reach equilibrium after a brief period of time of exposure to air. The present results suggest that the oxide layer continues to change long after deposition.

In order to consider the effect of growth rate and Si/Al ratio, Si films with thickness of 2-3 μm was deposited by HWCVD at 5 μm/hr at 430°C on Al layers 100, 250, 500 and 1000 nm thick. Optical micrographs taken through the glass substrate of the Si films showed large areas of polycrystalline Si grains. The central area of the film on 500 nm Al, appears to have the densest coverage approaching 100%. The edge areas of this film had a low fractional formation of Si grains. However, after the 8 hr post deposition anneal at 500°C, the edge area had a similar high fractional coverage as the middle.

These continuous polycrystalline layers appear as promising candidates for device fabrication.

It has been reported that the aluminum oxide layer is required for the layer exchange process, although it is not required for the crystallization process itself. It also acts as a diffusion barrier for Si and Al atoms leading to a lower nucleation and thus large Si grains. The growth of the oxide represents a potentially uncontrolled variable in much of the MIC work. The oxide surface of Al films was monitored over a period of 12 days using spectroscopic ellipsometry (SE) measurements. Samples of e-beam deposited Al on glass were stored in air. Although formation of the native oxide layer is thought to be a self-limiting process, SE reveals changes in the optical properties of the oxide layer over the 12 days indicating that its structure may be changing long after the Al film deposition.

Previously, we have reported that such high temperature Si deposition on Al was problematic since the Al films appear to become discontinuous. Recently, it was found that Al films heated to 600°C in vacuum remained continuous. Buffer layers between the glass and Al will be studied to see if they can maintain wetting on the glass, hence, give continuous Al films with Si film deposition at T>600°C.

Regarding solar cell development, we have worked on solving dopant cross contamination in our PECVD system and on developing B doped HWCVD layers for use as an absorber for a thin film Si device. Recently, a-Si devices fabricated in the single chamber PECVD reactor had lower fill factors compared to devices fabricated several years ago. QE analysis indicates that the lower FFs are caused by poor hole collection in the i-layer, most likely arising from donor impurities such as P or O. We were concerned about cross-contamination since the PECVD system will be needed for deposition of thin a-Si n and i layers for HIT-type emitters on the HWCVD p-type base layer. Several a-Si i-layers and devices were sent to NREL for SIMS characterization. Concentrations of the atmospheric contaminants N and C in the i-layer of all samples were low and comparable in magnitude, and relatively uniform in distribution, suggesting that air leaks are not responsible. For most samples, the P concentrations were below the c-Si background level. But a recent sample, having low FF, had double the O concentration compared to the earlier ones. This sample was the only one to have measurable P contamination. Several PECVD device runs were made with varying burying layer, bake-out procedures, and p-layer flows. Bias dependent QE measurements showed a very clear dependence on the p-layer gas flow conditions. The data is consistent with the longer p-layer contributing more B dopant incorporation in the i-layer, which was not removed by our standard p-i interface pump/purge cycle and a-SiC buffer layer, thus leading to poor electron collection. Improved burying layers and reduced p-layer B flow will be investigated to control and reduce cross-contamination.

The deposition of boron doped HWCVD Si films was investigated as part of our effort to develop polycrystalline thin film Si devices. The films were deposited at 500 m Torr and 450 °C with B_2H_6/SiH_4 flow ratios varying from 10^{-5} to 10^{-3}. For all dopant gas concentrations, the resulting dark conductivity of the films was 10^{-6} S/cm. In order to

understand whether the invariance in conductivity was the result of the deposition conditions or film structure, doped films were deposited with varying thickness. Increasing the thickness by a factor of 3 increases the conductivity by 2 orders of magnitude but did not change the activation energy, indicating an increase in mobility with thickness.

4.4 Phase 4 Summary: 9/5/04 to 9/4/05

Aluminum-induced crystallization (AIC) of Si thin films on glass substrates was investigated as potential techniques leading to continuous large grain Si films. Silicon films were deposited by Hot-Wire Chemical Vapor Deposition (HW-CVD), Plasma Enhanced Chemical Vapor Deposition (PE-CVD) and Electron beam deposition (E-beam) onto Al coated Corning 7059 glass substrates and the annealing of the samples was performed at temperatures below the eutectic temperature of Si-Al binary system (577^{o}C). Both in-situ and ex-situ AIC was evaluated. The grain structure of the polycrystalline silicon (poly-Si) films formed on glass substrates and Al-Si interface were studied by various analytical techniques. Continuous poly-Si films were obtained using Al layers with a thickness of 500 nm or less, and with a Si/Al thickness ratio of at least 1. The average grain size of poly-Si films was affected by the a-Si deposition technique. E-beam deposited a-Si films resulted in 10-15 μm average grain size while PECVD and HWCVD deposited a-Si films resulted in slightly smaller grain sizes. The nature and morphology of the interface oxide layer between Al and Si layers was studied by XPS and were found to be crucial for layer exchange process. The length of time that the Al layer was exposed to air was used to vary the oxide thickness. The effective activation energy for the ex-situ crystallization and layer exchange process was determined to be 0.9 eV.

Continuous poly-Si films on glass substrates were obtained using an *in-situ* aluminum-induced crystallization technique at 430^{o}C. The 0.5 μm Al film was deposited by e-beam and the 0.6 μm Si deposited by HWCVD. Poly-Si films had an average grain size of 10-13 μm, corresponding to a grain size/thickness ratio greater than 20 and similar to poly-Si films prepared by conventional AIC. A unique etching procedure was developed involving repeated cycles of alternately etching the Al then the Si to reveal the continuous Si layer below. Poly-Si layers prepared by either an in-situ or conventional AIC process can be used as seed layers for epitaxial Si growth or for back contact formation in c-Si solar cell fabrication at temperature below 500^{o}C. As an alternative to conventional AIC, the in-situ AIC process eliminates an additional annealing step, which saves considerable time during processing.

4.5 Phase 5 Summary: 9/5/05 to 3/31/07

Aluminum induced crystallization (AIC) of electron beam evaporated amorphous silicon on two substrates, Corning-1737 glass and (100) oriented single crystalline silicon wafer, was evaluated at annealing temperatures below 450^{o}C, and above 600^{o}C, eutectic temperature (EuT), with stacking structure of an a-Si/Al/substrate. Samples were

analyzed with optical microscopy, X-ray diffraction, Raman spectroscopy, scanning electron microscopy and energy dispersive spectrometer. For samples grown on glass substrates, continuous crystalline silicon films with grain size of ~ 30μm have been achieved below EuT, while discontinuous crystalline Si "islands" are formed above EuT. For samples grown on Si wafer, no crystallization has been observed below EuT; while above EuT, AIC process occurs with a non-uniform crystalline silicon network formed on the top of the wafer. The crystallized Si films on glass substrate annealed below EuT can be useful as very conductive P-type seed layers for subsequent epitaxial thickening for thin crystalline silicon solar cells on low cost substrates.

Heterojunction c-Si solar cells utilizing a-Si emitters, contacts, and passivation layers have demonstrated high V_{OC} but often with low FFs (S-shape curve). The problem of maintaining high V_{OC} without a loss in FF was studied intently at IEC and was finally solved, leading to an NREL confirmed 17.7% efficiency with V_{OC} =.654 V, FF=76%, and J_{SC}=35.7 mA/cm^2.

We have also developed a new structure of an all back contact solar cell incorporating silicon heterojunctions. This structure has interdigitated p/n amorphous silicon (a-Si:H) films deposited by plasma-enhanced chemical vapor deposition on the backside of crystalline silicon (c-Si) wafers, with the light irradiating the front surface. Interdigitated back contact Si heterojunction (IBC-SHJ) cells possess advantages over front junction a-Si:H/c-Si heterojunction cells due to minimized current losses in the illuminating side, and over traditional diffused back-junction cells due to low temperature processing combined with the potential of high voltages for the heterojunction. Devices were fabricated on 300 μm thick, polished, n-type float-zone silicon wafer with resistivity of 2.5 Ωcm. The front surface is presently passivated with an intrinsic a-Si:H layer of 20 nm thick deposited by DC plasma enhanced chemical vapor deposition (PECVD) system at 200°C. At the back side of wafer, the contacts are provided by alternating strips of n and p-type interdigitated a-Si:H layers at a thickness of 20 nm. The interdigitated pattern was created by two-step photolithography. The finger-like p-region has lateral dimension of 1.2 mm, while n-region is 0.5 mm wide. The separation between p- and n-regions is ~2 μm, and is formed naturally by undercutting during the etching process. Initial IBC-SHJ cell structures made at IEC have achieved NREL-confirmed cell efficiencies of 11.8% under AM1.5 illumination. We have measured V_{OC}'s of 680 mV.

Device results (JV, QE, and lifetime) indicated a strong light intensity dependence. The lowering of the surface recombination velocity as the carrier density increases is due to saturation of the recombination centers. With increasing the illumination level, the carrier density rises dramatically, saturating the recombination centers and increasing the measured minority carrier lifetime. Annealing was found to improve performance of the IBC-SHJ. Fourier transform infrared spectroscopy indicated that bonds at a-Si/c-Si interface are transformed from dihydride to monohydride after annealing. The lowering of defects in the a-Si layer reduces the surface recombination velocity. It was found that the original lifetime 500μs increases to >1ms after annealing.

4.6 Phase 6 Summary: 4/1/07 to 12/31/07

The Si effort has been directed towards fabricating, characterizing, and modeling Si solar cells based on n-type Cz wafers with deposited contacts and emitters with the goal of improving V_{OC}. Studies of deposition, structure and electrical properties of thin PECVD Si layers combined with "effective lifetime" measurements, and heterojunction modeling has given insight into mechanisms responsible for improving the effective Si wafer surface passivation.

Silicon surface passivation of hydrogenated silicon (Si:H) thin films deposited by radio frequency (RF) and direct current (DC) plasma process was investigated by measuring effective minority carrier lifetime (τ_{eff}) on Si (100) and (111) wafers and correlated with the silicon heterojunction (SHJ) cell performances. Apparently the higher ion bombardment in DC compared to RF plasma during growth of a-Si (a-Si:H) layer does not deteriorate Si surface passivation properties. Microstructural defects associated with SiH_2 bonding have only a weak influence on τ_{eff}. However, any epitaxial growth or presence of crystallinity in the Si:H i-layer severely degrades passivation properties and SHJ cell performance. Excellent surface passivation (τ_{eff} > 1 msec) and high efficiency SHJ cells are obtained by both RF and DC plasma-deposited intrinsic a-Si:H buffer layer. High efficiency (>18%) with open circuit voltage (V_{OC}) of 694 mV was achieved on n-type textured Cz wafer using DC plasma process.

Interpretation of photovoltaic cell performance through current-voltage testing depends largely on accurate representation of the band structure. This is especially true when considering the numerous interfaces found in a silicon heterojunction (SHJ) cell comprised of deposited a-Si:H emitter, passivation layers, and back contact with a crystalline silicon (c-Si) wafer absorber. Therefore, we determined the electronic levels of the valence and conduction bands, Fermi position, and electron affinity of thin film p-, i-, and n-type a-Si:H as well as (n)c-Si for use in SHJ modelling and performance optimization. Novel application of wet chemically H-terminated a-Si:H enables the study of device quality films to be studied via ultra-violet and X-ray photoemission spectroscopy. It is shown that this H-termination strategy effectively removes native oxide without introducing detectable surface states. The Fermi level varies within a bandgap of ~1.75eV from 1.3 – 0.70eV from the valence band maximum depending on doping and plasma conditions. The electron affinity is measured to be approximately 3.91eV for i-type films, 3.83 for n-type and a surprisingly low 3.37eV for p-type. Also the validity of Fermi level alignment of (p)c-Si/a-Si:H heterojunctions is called into question.

An interdigitated back contact silicon heterojunction solar cell has been developed. It combines the high voltage potential of heterojunction solar cells while avoiding the absorption losses in these structures which allows high short circuit currents. This structure has interdigitated p/n a-Si:H-films deposited by low temperature plasma enhanced chemical vapor deposition on the backside of crystalline silicon (c-Si) wafers, with the light irradiating the front surface. The device is attractive for manufacturing due to the all back contact design, the large tolerances in dimensions,

low temperature of depositions, and the lack of shunting. Initial solar cells have open circuit voltages of 691 mV but low fill factors. A device was measured at NREL with 11.8% efficiency. High shunt resistance is evidence that the emitter and contact remain isolated despite the relatively simple masking procedure. Two-dimensional modelling is used to explain the present low fill factors obtained with the intrinsic a-Si buffer layer and demonstrates that the structure allows efficiencies in excess of 24%. Very good agreement is shown between measurement of the spatial variation of an LBIC signal across the interdigitated emitter and contacts and the 2D model confirming the assumptions about the device operation and the material parameters used in the model.

Si TFP Team Activity and Industrial Collaboration

IEC continued support of Si wafer-based cell development at BP Solar. Deposition of various contact layers and characterization of optical, electrical and junction properties was carried out on their wafers. We assisted Advent Solar in evaluation of anti-reflection and passivation layers on their wafers as well.

Regarding a-Si based thin film PV companies, IEC is supporting Sencera and Sierra Solar in developing their process technology.

4.7 Phase 7 Summary: 1/1/08 to 5/31/08

Passivation of silicon surface with intrinsic a-Si:H

The passivation of crystalline silicon surfaces is necessary for high performance devices as the surfaces are areas of high recombination. Amorphous silicon (a-Si) has proved to be an effective passivation layer and here at IEC we have achieved voltages above 700 mV. The level of passivation is dependent on the structure of the deposited amorphous layer. A critical factor in the growth of silicon films is the ratio of hydrogen to silane flow rate denoted here as the R ratio, where a high R ratio indicates a large about of hydrogen dilution.

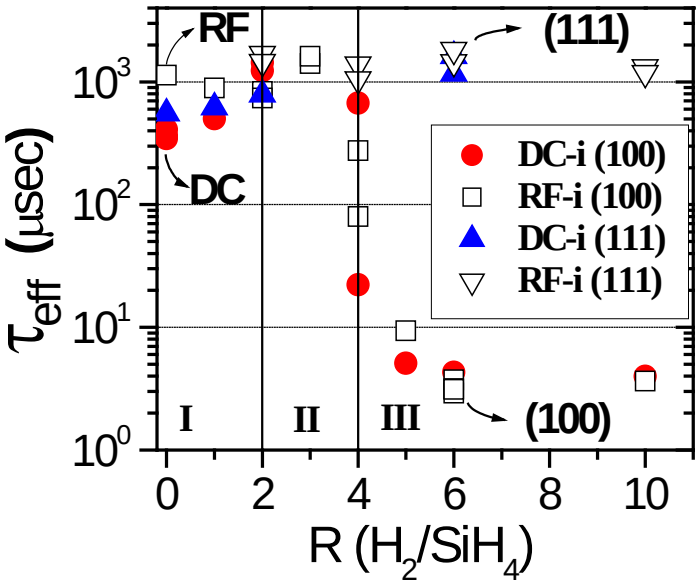
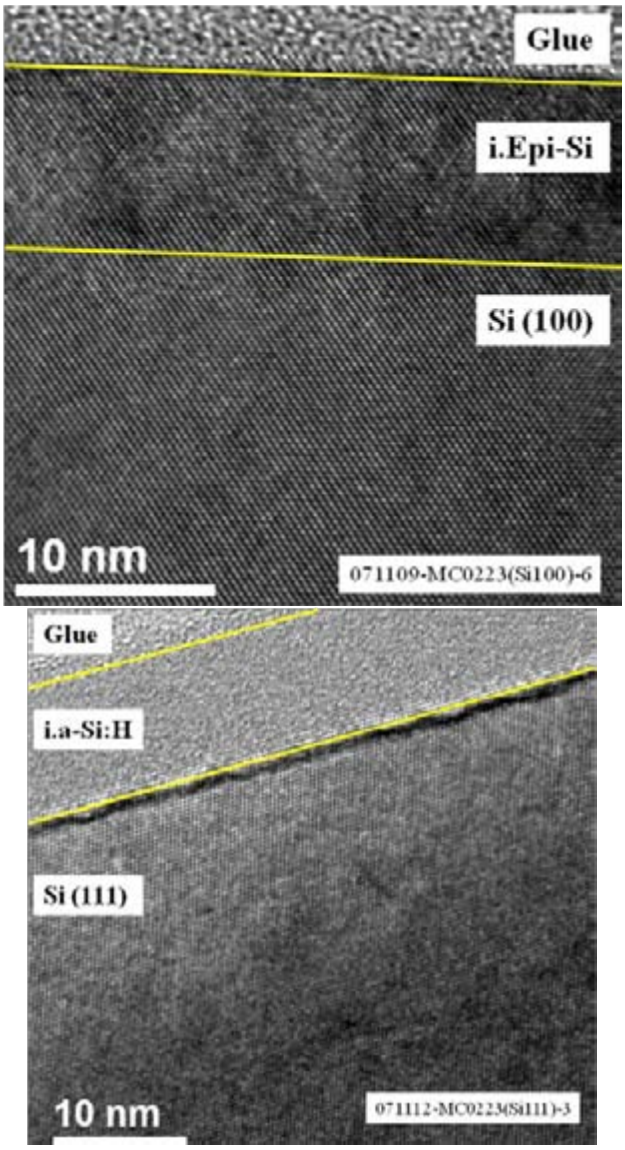


Figure 1. Effective minority carrier lifetime (τ_{eff}) on Si (100) and (111) wafers with 10 nm Si:H i-layer deposited on both sides by RF and DC plasma at variable hydrogen dilution (R).

Figure 1 shows τ_{eff} as a function of R for i-layers deposited on (100) and (111) wafers by DC and RF plasma after annealing the samples at 280°C for 10 mins. Three distinct regions can be identified in the variation of τ_{eff} with R. In region I, R < 2, τ_{eff} depends on the plasma process; namely, DC plasma deposited i-layers at R = 0 show slightly lower lifetime, ~ 500 μsec, than RF plasma deposited i-layers, > 1 msec, irrespective of the wafer surface orientation. τ_{eff}, however, becomes similar for RF and DC plasma deposited i-layers at R > 2, region II and III, implying little or no adverse effect of ion damage in the DC process on Si surface passivation. In region III, R > 4, the measured τ_{eff} exhibits a pronounced Si surface orientation dependence. The values of τ_{eff} sharply decrease to < 10 μsec on (100) wafers, while on (111) wafers they remain > 1 msec even at R = 10. In the following section, the DC i-layers are further examined using cross-sectional transmission electron microscopy (XTEM).

XTEM images of c-Si / a-Si:H interfaces

Figure 2 shows the deposition of a layer of silicon deposited by PECVD on polished crystalline silicon substrates. In image (a), the silicon layer shows a high degree of crystallinity with epitaxial growth so that there is not a clear interface between the substrate and the deposited silicon layer. The lifetime for this sample is low so that the surface is essentially unpassivated as shown in Figure 1 where the R6 lifetime on (100) is only 40 μs.



(a) **(b)**

Figure 2. TEM of R6 DC i-layer deposited on silicon substrates. (a) with a (100) orientation and (b) with a (111) orientation.

In contrast, the image of (b) shows a completely amorphous layer on top of the crystalline silicon substrate and the lifetime is well above 1 ms. The only difference between the two images is the substrate orientation. The (111) orientation has suppressed crystallinity leading to an amorphous film.

To understand the wafer orientation dependence of τ_{eff}, i-layer structure and optical properties are determined from VASE measurements on the same samples used for lifetime testing. Figure 3 shows the imaginary part of the pseudo dielectric constant, ε_2, as a function of photon energy (E) for i-layers deposited on (100) and (111) wafers at R = 6. A broad featureless spectrum for the R = 6 i-layer on Si (111) wafer is indicative of amorphous Si:H structure. However, the same Si:H layer deposited on (100) wafer exhibits the identical optical constants as crystalline silicon, which implies that the film is

epitaxial; this is confirmed by transmission electron microscopy (TEM). This indicates that any epitaxial growth of i-layers severely deteriorates the surface passivation quality of the deposited layer and τ_{eff} drops to less than 10 μsec (see Figure 1).

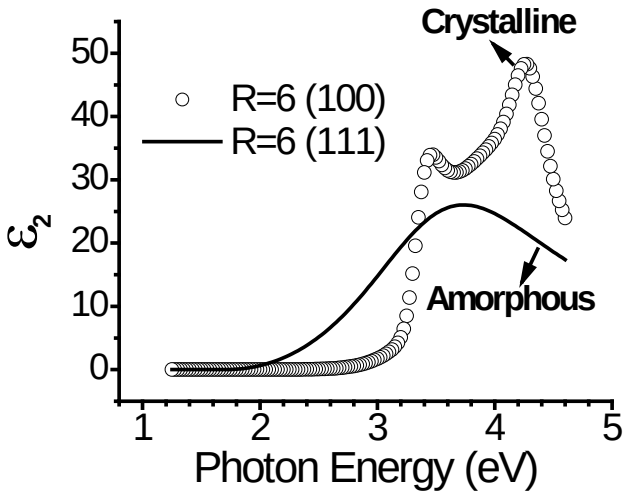


Figure 3. Imaginary part of pseudo-dielectric function (ε_2) as a function of photon energy (E) for the Si:H i-layers deposited with R = 6 on (100) and on (111) wafers.

Figure 4 shows the deposition of two layers as would be typical in a solar cell structure. An R6 i-layer followed by a p-type deposition passivates and forms a junction. In both cases the films are completely amorphous and we see no crystallinity forming with the thicker film. The other feature to note is that there is no interface layer between the i-layer and the crystalline silicon substrate as is evident in the previous image. The loss of interface layer is believed to be due to the further annealing that this layer has experienced over that of Figure 2(b).

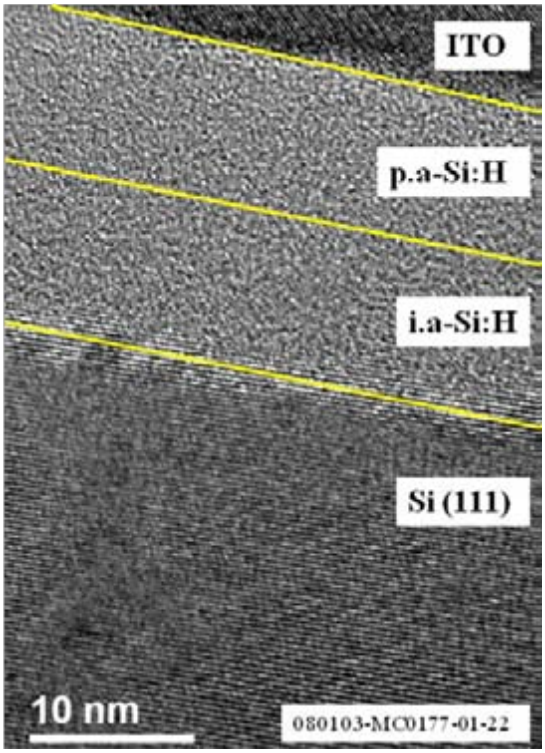


Figure 4. R6 DC i-layer and p-layer on (111) Si substrate.

The XTEM final image is for a deposition on (111) material where there is a very high dilution of the growth with hydrogen and R = 40. In this case we get the growth of a microcrystalline film on the substrate. The crystal structure of the film is very poor unlike that of Figure 2(a) where epitaxial growth was seen. The loss of amorphous film has caused a loss of passivation in this layer and the lifetime has dropped to under 100 μs.

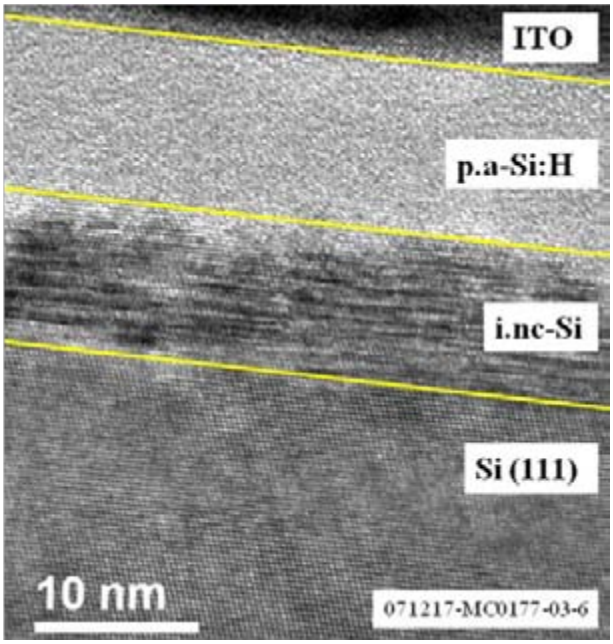


Figure 5. R40 DC i-layer and p-layer on (111) Si substrate.

The XTEM images show that good passivation and low surface recombination is only achieved with an amorphous film. Amorphous films grow more readily on (111) surfaces and by using layers with a lower hydrogen dilution.

Fabrication of Back Junction Devices

Figure 6(a) shows the schematic structure of the front silicon heterojunction (SHJ) and interdigitated back contact-silicon heterojunction (IBC-SHJ) cells. All the a-Si:H layers are deposited using identical plasma conditions in both cell structures. The i-layers are deposited with R = 2 to suppress the growth of microcrystalline silicon. The illuminated J-V curves are compared in Figure 6(b). The V_{OC} values (~690 mV) are the same in both structures, while J_{SC} is higher (~ 3 mA/cm^2) in the IBC structure due to reduced optical loss at the front illuminating side. However, the FF in this IBC structure is very low due to the "S" shape J-V curve. This result indicates the necessity of further optimization of IBC-SHJ solar cells. There are two major functional differences between the front-junction and IBC device structures: (i) the carrier transport is one dimensional in front-junction SHJ cell, while the IBC-SHJ structure has a two dimensional transport mechanism, and (ii) the front i-layer in front-junction SHJ cell gets illuminated and generates photo carriers, while the i-layer in the IBC structure is in the dark and does not generate carriers.

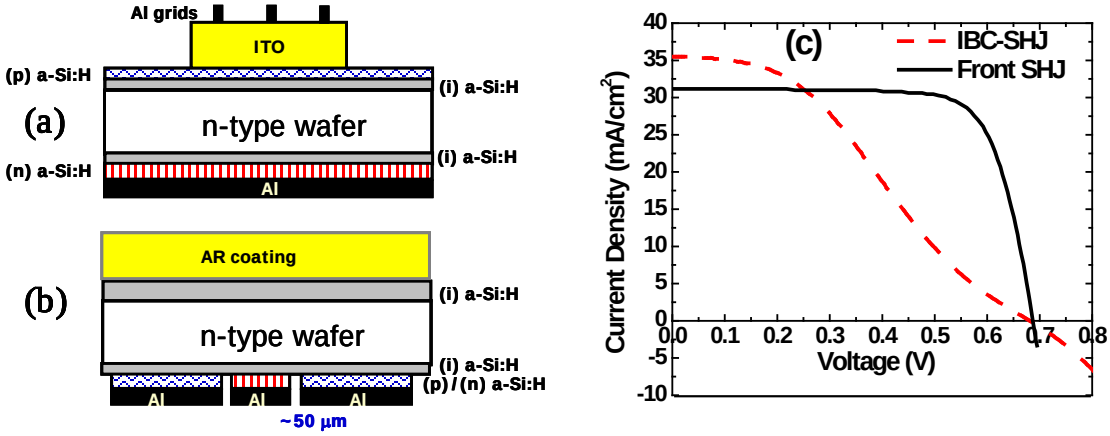


Figure 6. Schematic structures of (a) front junction SHJ cell, (b) IBC-SHJ cell, and (c) comparison of the illuminated J-V curves in two cell structures.

2D numerical simulation of IBC-SHJ solar cell

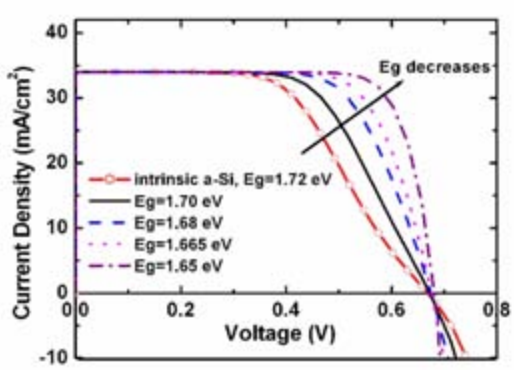
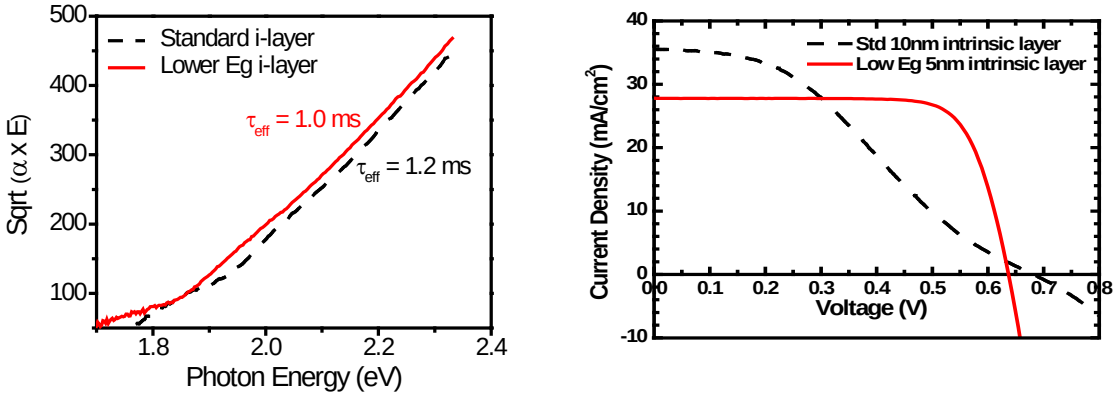


Figure 7. Simulated J-V curves for IBC-SHJ cells [structure shown in Figure 8 (b)] under illumination with variable band gap of the intrinsic a-Si buffer layer.

We have performed 2D numerical simulation using a "Sentaurus Device" simulator (called DESSIS in its old version). Both the experimental results and numerical simulation confirm that low FF with an "S" shape J-V appears in IBC-SHJ structure due to the presence of an intrinsic a-Si:H buffer layer only in the p-type emitter strip. This suggests the existence of a hole transport barrier across the intrinsic a-Si:H buffer layer.

The low FF and "S" shape J-V can arise from the hole transport barrier due to the enhanced valence band offset generated by the intrinsic buffer layer. Hence the effect of band gap of the intrinsic a-Si buffer layer on IBC-SHJ cell performance is studied. Again, the surface passivation effects of the different buffer layers are assumed to be the same, while electron affinities of the buffer layers are assumed constant. Figure 7 shows the illuminated J-V characteristics obtained from simulation for intrinsic a-Si buffers as a function of band gaps. A substantial effect of the band gap is evident on FF, which increases from 55% to >78% as the band gap of the buffer layer is reduced by 0.07 eV.

To simultaneously maintain high V_{OC} and J_{SC} with narrower band gap buffer layers, high passivation quality of the buffer layer is also required. Intrinsic a-Si:H buffer layers with narrower band gaps are developed by varying plasma process parameters without alloying with other semiconductors like Ge. Figure 8(a) shows the Tauc's plot for two different a-Si:H layers, where the dashed (black) curve represents the control buffer layer, and the solid (red) curve indicates the newly developed i-layer. It can be seen that the band gap of the new i-layer is ~0.04 eV narrower than that of the control layer. The τ_{eff} values shown beside the curves indicate that they have similar passivation quality. Figure 8(b) compares the illuminated J-V curves for the IBC-SHJ cells with 5 nm narrower band gap i-layer and 10 nm higher band gap i-layer. An IBC-SHJ cell with efficiency of 13.5% and FF of 77% is achieved with the narrower band gap i-layer. However, the V_{OC} and J_{SC} is lower than the standard i-layer, which is due to insufficient surface passivation in the gap between the p- and n- strips.



(a) **(b)**

Figure 8. (a) Tauc's plot for control (black dashed curve) and newly developed (red solid curve) intrinsic a-Si:H layers, and (b) illuminated J-V curves of IBC-SHJ cells with a 5 nm lower band gap i-layer and 10 nm standard i-layer.

5 IN-LINE DIAGNOSTICS AND PROCESS CONTROL

5.1 Phase 1 Summary: 9/5/01 to 9/4/02

Widespread use of photovoltaic technology is hindered by its high costs. One of the most promising strategies for lowering PV costs is the use of thin film technologies in which the PV materials are deposited onto inexpensive large area substrates such as window glass and flexible substrates. Benefiting from the inherent advantages to thin film PV will require breakthroughs in reducing manufacturing costs, primarily by improving yields and increasing throughput. A critical requirement to improve manufacturing yields is the development diagnostics tools and associated predictive models that quantitatively assess processing conditions and product properties. Incorporation of the diagnostic sensors into both laboratory reactors and manufacturing facilities will: 1) underpin the development of solar cells modules with improved efficiency; and 2) accelerate the scale-up process through model-base process control schemes. In-situ, in- line diagnostics tools are needed for process and product quality control, as well as, non-destructive testing for off-line product evaluation. Currently, diagnostic capabilities required for manufacturing large area thin film modules are in their infancy and all thin-film manufacturers can only assess their product after completion of the module.

Under this task, a preliminary survey of available sensor technologies was performed which focused primarily on product diagnostics to evaluate film properties such as thickness, composition, crystallinity and grain size, and optical bandgap and changes structural and chemical changes during processing. The sensors consider where ellipsometry, X-ray diffraction/fluorescence, and infrared spectroscopy techniques as well as atomic absorption spectroscopy as a process control sensor.

5.2 Phase 2 Summary: 9/5/02 to 9/4/03

Contact wetting angle, ellipsometry and glancing incidence x-ray diffraction are surface sensitive technique methods that are under investigation as diagnostic tools for thin-film processing. An apparatus for carrying out contact angle measurements was constructed and wetting angle measurements are being carried out on different types of samples to determine the sensitivity to changes in surface energy arising from thin-film processing. Ellipsometry is being developed to determine film composition in multi-layer thin-film structures such as treated CdTe surfaces. Glancing x-ray diffraction is being developed to determine residual stress in thin films and the thickness of surface layers obtained on CdTe films under different post-deposition processing conditions and to evaluate residual stress in as-deposited Mo films.

5.3 Phase 3 Summary: 9/5/03 to 9/4/04

The in-line process diagnostic effort is intended to develop the tools needed for process control and quantitative models to link sensor output to process variables to material properties. Commercial-scale PV module fabrication would benefit from methods to analyze thin-film surfaces at various stages of processing. Contact wetting angle measurement is a simple diagnostic tool that may be suitable in industrial applications for monitoring changes in thin film solar cell processing conditions.

The terminating surface of a solid is known to contain excess free energy when compared to the bulk. Surface energies (E^P) consist of polar energies (E^D) resulting from permanent and induced dipole moments as well as hydrogen bonding, and dispersive energies that arise from vibrational interactions between atoms. The interaction of liquids and solids of different surface energies are known to give rise to the formation of characteristic angles known as wetting angles at a liquid/solid interface.

Wetting angles were recorded for water droplets deposited onto CdTe surfaces at varying times over the course of an hr immediately (<1 min) upon removal from the evacuated deposition chamber, during exposure to air and after subsequent chemical etching for 5 sec. in a bromine-methanol solution. A CdTe film tested upon removal from the deposition chamber (as-dep) nearly completely wet the entire surface of the sample (θ ~1^o). Rapid increases in this value were observed over the first hr. Bromine-methanol etched films, however, experienced differing effects with respect to the magnitude of the wetting angle, which increased rapidly during the first 20 min then subsequently decreased nearly as swiftly implying that etching does not produce surfaces similar to that of as-deposited CdTe. The rate of change in wetting angles was greatest within the first hr of exposure to the atmosphere for both as-deposited and etched CdTe. $CdTeO_3$ is the predominant native oxide of CdTe. Changes in the magnitude of wetting angle can therefore be attributed to the formation of the native oxide $CdTeO_3$ for as-dep CdTe and in-part for the etched CdTe. For etched CdTe it is hypothesized that initially a thin amorphous Te layer is generated which begins to crystallize over a twenty-min period and then subsequently oxidizes to TeO_2, the predominant native oxide for Te.

The results of processing on the surface energies of PVD CdTe were studied. The oxides that are formed or removed as a result of processing primarily affect E^p leaving E^d largely unchanged, however, contact wetting was unable to differentiate between the formation of different oxide phases. Surface oxidation resulting from $CdCl_2$ treatment increased E^p, by 9.8, 8.7, and 5.9 mN/m for vacuum, dry air, and saturated air stored samples, respectively. Etching in Br_2:CH_3OH reduced E^p by 4.4, 16.8, and 9.6 mN/m due to the removal of oxides from the film surfaces for vacuum, dry air, and saturated air stored samples, respectively.

Effects of crystallization of ITO were evaluated for atmospheres containing air and argon. Energy changes may be attributed to higher surface polarity associated with the alignment and organization of bonds from previously amorphous states.

Thus, contact wetting is a simple and effective tool that is able to detect changes in surface energies resulting from post deposition processing. As-deposited CdTe seeks to satisfy dangling bonds through reaction with air ambient. Significant native oxidation of PVD (111) CdTe occurs within hours upon exposure to the atmosphere and can be observed by increases in wetting angles. Dry air storage of CdTe prior to $CdCl_2$ heat treatments forms beneficial (CdO) oxides while films kept in saturated air produce electronically detrimental $CdTe_2O_5$ on surfaces. Polar energies increase as a result of oxides formed during treatment and decrease upon removal via chemical etching.

5.4 Phase 4 Summary: 9/5/04 to 9/4/05

A wide range of thin film analyses using GIXRD were surveyed for implementation into thin film PV device fabrication as a diagnostic and monitoring tool. Construction of a hot stage allowed *in-situ* detection of CdTe surface oxidation and CdTe-CdS interdiffusion. The oxidation studies were complimented by compositional depth profiling by XPS using the system installed in 2005. Te film thickness on etched CdTe was determined by regression of a layer model with measured data at different incident beam angles. A unique solution is facilitated by considering primary beam attenuation in the Te film. Dual-axis GIXRD measurements of multiple (hkl) reflections allowed determination of depth-distribution of residual stress in sputtered Mo films. For ultra-thin CdS films with nanometer size particulates, the particulate size was determined by fitting the GIXRD line profile and evaluating the integral line breadth. Alloy distribution in $CuIn_{1-x}Ga_xSe_2$ films was determined by modeling GIXRD patterns obtained at different incident beam angles and verified by measuring a $CuIn_{1-x}Ga_xSe_2$ film from both sides. This methodology is being used to investigate reaction pathways for obtaining films with uniform composition and could be used as a product sensor in a developed process.

5.5 Phase 5 Summary: 9/5/05 to 3/31/07

Elemental sources used in $CuInGaSe_2$ thin film deposition process have been investigated and characterized for the purpose of developing rules to facilitate the process scale-up. Finite-element-based thermal modeling on the linear source-boat using the COMSOL Multiphysics software package showed that there is a temperature gradient along the source. The temperature was found to be cooler on the end where heater leads are connected. Thermocouple location that best estimates melt surface temperature was obtained through FEMLAB thermal simulation. Furthermore, properly placed thermocouples were shown to give accurate melt surface temperature independent of the melt level in the source. In an experiment, melt temperatures were then estimated along the operating Cu source through the thermocouples placed accordingly. The melt temperature did show the similar non-uniformity as was obtained from finite-element modeling. The non-uniformity was also observed in the Cu film thickness deposited on a substrate placed along the source. In addition, Direct Simulation Monte Carlo Technique was used to develop a more refined estimation of the effusion rates and flux distribution from the sources.

5.6 Phase 6 Summary: 4/1/07 to 12/31/07

Process diagnostics are critical to evaluate and monitor the processing of thin film solar cells to maintain yield and avoid a large amount of off-spec production. To implement process diagnostics in real time requires both process and product monitoring as well as process control. Previous reports have contained our work on using contact wetting angle and X-ray diffraction as process monitors. During this period, graduate student Kapil Mukati completed his dissertation, "An alternative structure for next generation regulatory controllers and scale-up of Cu(InGa)Se_2 thin film co-evaporative physical vapor deposition process" awarded by the Department of Chemical Engineering for research conducted at IEC under the direction of Drs. Birkmire and Eser. It describes the process control needed to implement in-line real-time process diagnostics. A summary of that research is contained here. Further details may be found in his dissertation.

Process control systems have three key performance attributes: Set-point tracking (T) is ability to cause the process output to follow set-point changes rapidly and faithfully; Disturbance rejection (D) is the ability to counteract the effects of external disturbances; and Robustness (R) the ability to remain stable and perform well in the face of inevitable plant/model mismatch. A controller whose tuning constants are related directly to these performance attributes will have definite advantages over other controllers. However, the popular PID controller, even though simple, has an intrinsic structure that results in a complicated, hence non-transparent, relationship between its tuning parameters and the three controller performance attributes, limiting the controller's achievable performance and making tuning more complex than necessary. In order to overcome the weaknesses of the PID controller, we have developed an alternative regulatory controller [the Robustness, Tracking, Disturbance rejection, and overall Aggressiveness (RTDA) controller] having the following salient features: it requires precisely the same information that is required for tuning PID controllers; its tuning parameters are directly related to the three key controller attributes of R, T, and D [an auxiliary fourth parameter, influences the overall controller aggressiveness (A)]; all four tuning parameters are normalized to lie between 0 and 1; and the magnitude of a tuning parameter is related to performance aggressiveness, where the higher magnitudes signify conservative performance in the attribute of interest. In addition, the proposed predictive controller is not any more complicated to implement, in either software or hardware, than the PID controller.

In order to study how the choices of various RTDA controller parameter values jointly and individually affect closed-loop stability, a theoretical robust stability analysis is performed. The results of this analysis are subsequently used to develop systematic strategies for choosing the RTDA controller parameters that provide the best possible trade-off between robust stability and performance. The design and implementation of the RTDA controller in practice are illustrated experimentally using two processes: a lab-scale four-tank process with time delay and a pilot-scale physical vapor deposition process with nonlinear dynamics. These experiments demonstrate the RTDA controller's

improved performance over PID controllers. The RTDA control scheme is also extended to integrating and open-loop unstable processes.

A pilot-scale co-evaporative physical vapor deposition (PVD) process for manufacture of copper indium gallium diselenide ($Cu(InGa)Se_2$) thin films is chosen to validate the proposed RTDA controller experimentally, since robust control of film thickness and composition set-points for long deposition times cannot be achieved without effective base regulatory control. However, unlike film thickness and composition *set-points* that can be achieved with proper process *control*, achieving film thickness *uniformity* across large area substrates is a process *design* issue. To achieve good process performance, the process design issues are addressed first, and then the regulatory controller design is improved.

The work presented in Part II of this thesis is focused mainly on the evaporation source design. Such a study requires not only the detailed knowledge of the evaporation source temperature profile, but also accurate estimation of nozzle flow properties (effusion rates and vapor flux distribution). A three-dimensional first-principles electro-thermal model of the source is developed using the COMSOL Multiphysics^{TM} finite-element method, and the Direct Simulation Monte Carlo (DSMC) technique is employed to predict accurately the nozzle flow properties for any given nozzle geometry and evaporant. These models are validated experimentally, and subsequently used to design evaporation sources that not only achieve the targeted film thickness uniformity, but also maximize the material utilization efficiency. Results of this work were reported in IEC's previous annual report.

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2008

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"$Cu(InGa)Se_2$ Film Formation from Selenization of Mixed Metal./Metal-selenide Precursors," Rui Kamada, William Shafarman, Robert Birkmire

"High Throughput Processing CdTe/CdS Solar Cells with Thin Absorber Layers," Brian McCandless and Wayne Buchanan

"Cross-Section Potential Analysis of CdTe/CdS Solar Cells by Kelvin Probe Force Microscopy," Brian McCandless and Sergey Rykov

"Control of Composition in Co-evaporated $Cu(InGa)(SeS)_2$ Thin Films," Shiro Nishiwaki, Greg Hanket, Robert Birkmire and William Shafarman

"Temperature Dependence of V_{OC} in CdTe and $Cu(InGa)(SeS)_2$-based Solar Cells," Christopher Thompson, Steven Hegedus, William Shafarman and Darshini Desai

"In-situ Annealing of $Cu(InGa)Se_2$ Films Grown by Elemental Co-evaporation," James Wilson, Robert Birkmire and William Shafarman

"Properties of Encapsulated CIGS Cells in 85ºC/85%RH," Larry C. Olsen, Mark E. Gross, Sambhu N. Kundu, and William N. Shafarman

"Band Gap Energy of Chalcopyrite Thin Film Solar Cell Absorbers Determined by Soft X-ray Emission and Absorption Spectroscopy," M. Bar, L. Weinhardt, S. Pookpanratana, C. Heske, S. Nishiwaki, W.N. Shafarman, O. Fuchs, M. Blum, W. Yang and J.D. Denlinger

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"The Influence of Sodium on Metastable Defect Kinetics in CIGS Materials," Peter T. Erslev[a], Jin Woo Lee[a], J. David Cohen[a] and William N. Shafarman[b]
[a]University of Oregon Physics Department, Eugene, Oregon, USA
[b]Institute for Energy Conversion, University of Delaware, Newark, Delaware, USA

Applied Physics Letters

"Electronic Level Alignment at the Deeply Buried Asborber/Mo Interface in Chalcopyrite-based Thin Film Solar Cells,"
M. Bär*, L. Weinhardt, S. Pookpanratana, and C. Heske - Department of Chemistry, University of Nevada, Las Vegas
S. Nishiwaki and W.N. Shafarman - Institute of Energy Conversion (IEC), University of Delaware – submitted May 2008

Physical Review B

"CHEMICAL STRUCTURE OF THE $Cu(In,Ga)Se_2$/Mo AND $Cu(In,Ga)(S,Se)_2$/Mo INTERFACES,"
M. Bär, L. Weinhardt, and C. Heske
Department of Chemistry, University of Nevada, Las Vegas (UNLV
S. Nishiwaki and W. N. Shafarman
Institute of Energy Conversion (IEC), University of Delaware – submitted April 2008.

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14. ABSTRACT *(Maximum 200 Words)*

This report describes results achieved under this subcontract to develop and understand thin-film solar cell technology associated to CuInSe2 and related alloys, a-Si and its alloys, and CdTe. This includes application of a-Si to c-Si wafer-type cells, as well. Modules based on all these thin films are promising candidates to meet DOE long-range efficiency, reliability, and manufacturing cost goals. The critical issues being addressed under this program are intended to provide the science and engineering basis for developing viable commercial processes and to improve module performance. The generic research issues addressed are: 1) quantitative analysis of processing steps to provide information for efficient commercial-scale equipment design and operation; 2) device characterization relating the device performance to materials properties and process conditions; 3) development of alloy materials with different bandgaps to allow improved device structures for stability and compatibility with module design; 4) development of improved window/heterojunction layers and contacts to improve device performance and reliability; and 5) evaluation of cell stability with respect to illumination, temperature, and ambient and with respect to device structure and module encapsulation.

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