ARMY RESEARCH LABORATORY



Effects of Differing Carbon Nanotube Field-effect Transistor Architectures

by Andrew M. Dorsey and Matthew H. Ervin

ARL-TR-4883 **July 2009**

Approved for public release; distribution unlimited.

NOTICES

Disclaimers

The findings in this report are not to be construed as an official Department of the Army position unless so designated by other authorized documents.

Citation of manufacturer's or trade names does not constitute an official endorsement or approval of the use thereof.

Destroy this report when it is no longer needed. Do not return it to the originator.

Army Research Laboratory
Adelphi, MD 20783-1197

ARL-TR-4883 **July 2009**

Effects of Differing Carbon Nanotube Field-effect Transistor Architectures

Andrew M. Dorsey and Matthew H. Ervin
Sensors and Electron Devices Directorate, ARL

Approved for public release; distribution unlimited.

REPORT DOCUMENTATION PAGE	Form Approved OMB No. 0704-0188

Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing the burden, to Department of Defense, Washington Headquarters Services, Directorate for Information Operations and Reports (0704-0188), 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302. Respondents should be aware that notwithstanding any other provision of law, no person shall be subject to any penalty for failing to comply with a collection of information if it does not display a currently valid OMB control number.

PLEASE DO NOT RETURN YOUR FORM TO THE ABOVE ADDRESS.

1. REPORT DATE *(DD-MM-YYYY)*	2. REPORT TYPE	3. DATES COVERED (From - To)
July 2009	Final	May 2007 to December 2008

4. TITLE AND SUBTITLE

Effects of Differing Carbon Nanotube Field-effect Transistor Architectures

5a. CONTRACT NUMBER

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)

Andrew M. Dorsey and Matthew H. Ervin

5d. PROJECT NUMBER

5e. TASK NUMBER

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

U.S. Army Research Laboratory
ATTN: RDRL-SER-L
2800 Powder Mill Road
Adelphi, MD 20783-1197

8. PERFORMING ORGANIZATION REPORT NUMBER

ARL-TR-4883

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

10. SPONSOR/MONITOR'S ACRONYM(S)

11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT

Approved for public release; distribution unlimited

13. SUPPLEMENTARY NOTES

14. ABSTRACT

Single-walled carbon nanotube field-effect transistors (SWCNTFETs) were fabricated with varying device architectures. Variations on the standard back-gated architecture included varying the gate oxide material and thickness, changing source and drain contact metallization, suspending the carbon nanotubes to minimize interaction with the gate oxide, and fabricating a top-gated architecture employing a thin layer of aluminum oxide (Al_2O_3) as the gate oxide. Devices were characterized and compared to each other based on the CNTFET properties of noise, hysteresis, sub-threshold slope, and threshold voltage. Results show that some properties of the CNTFET, such as hysteresis and noise can be modified; other properties, however, are intrinsic to the CNT.

15. SUBJECT TERMS

CNTFET

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			Matthew H. Ervin
Unclassified	Unclassified	Unclassified	UU	22	19b. TELEPHONE NUMBER (*Include area code*) (301) 394-0017

Standard Form 298 (Rev. 8/98)
Prescribed by ANSI Std. Z39.18

Contents

List of Figures iv

1. Introduction/Background 1

2. Experiment/Calculations 1

2.1 CNT Growth and Deposition 1
2.1.1 CVD Growth 1
2.1.2 CNT Solution Deposition 3
2.2 Device Processing 4
2.2.1 Back-gated CNTFETs with Differing Gate Oxides 4
2.2.2 Back-gated CNTFETs with Differing Contact Metallizations 4
2.2.3 Top-gated CNTFETs 4
2.2.4 Suspended CNTFETS 5

3. Results and Discussion 6

3.1 Maximum and Minimum Source Current 6
3.2 Noise 8
3.3 Hysteresis 9
3.3.1 Back-gated CNTFETs with Differing Gate Oxides 9
3.3.2 Top-gated CNTFETs 10
3.3.3 Suspended CNTFETs 10

4. Summary and Conclusions 12

5. References 13

List of Symbols, Acronyms, and Abbreviations 15

Distribution List 16

List of Figures

Figure 1. a) Multiple SEM images stiched together of an extremely long SWCNT and b) zoomed out picture of the SWCNT better displaying its actual length. 2

Figure 2. a) Meshes of CNTs on the edge of a substrate, b) multiwalled CNTs mixed in with SWCNTs, c) aluminum oxide substrate with no CNTs visible, and d) high magnification image of nanoparticular aluminum oxide. 3

Figure 3. a) Top-gated CNTFETS, with interdigitated source/drain (lower) and gate (upper) electrodes; the source/drain gaps have unwanted CNTs, which are not overlapped by the gate. b) Optical microscope image of patterned resist for the selected removal of CNTs that are outside of the electrode overlap area.....5

Figure 4. a) Back-gated CNTFET sample before CNT suspension with a gate oxide etch. b) CNT suspended between source and drain contacts after vapor phase HF etch.....6

Figure 5. Cross sectional drawings of: a) a typical back-gated CNTFET, and b) a suspended CNTFET with fully and partially suspended tubes shown. 6

Figure 6. CNTFET after palladium deposition a) before anneal and b) after anneal. 8

Figure 7. a) Metallic CNT burnoff process for the palladium CNTFET shown in figure 6. b) Resulting CNTFET after all conditioning steps.....8

Figure 8. a) Comparison showing SNR increase after an anneal of the CNTFET. b) Comparison showing SNR higher on average for SiO_2 devices than for parylene devices. 9

Figure 9. a) Comparison showing hysteresis change with reduced gate voltage ranges. b) Example of a single tube device grown on 1300 Å SiO_2.....10

Figure 10. Source, drain, and gate characteristics for a gate voltage sweep of a top-gated CNTFET. 11

Figure 11. a) Comparison before and after vapor phase HF etch on suspension sample for a ±20 V gate sweep. b) Comparison for a ±10 V gate sweep.....11

1. Introduction/Background

Carbon nanotubes (CNTs) have received a lot of recognition as a potentially revolutionary component for future devices, based on their attractive material and electric properties. One device fabricated with CNTs that has been highly examined is the carbon nanotube field-effect transistor (CNTFET), comprised of single-wall CNTs (SWCNTs) as the active element between two metal source and drain contacts. Even though there are many advantages to the CNTFET, such as size, high sub-threshold slope, and low power consumption, the device still has its drawbacks—hysteresis and high threshold voltage, for example. The goal of this project is to investigate the effects of CNTFET device architectures on transistor performance as opposed to the effects of the CNT chirality (the orientation of the carbon atom lattice in the nanotube) (*1*). This involves CNTFET fabrication with different gate oxide materials and thicknesses, and alternative source-drain contact metallization layers, as well as experimenting with top-gated versus back-gated architectures.

2. Experiment/Calculations

2.1 CNT Growth and Deposition

2.1.1 CVD Growth

Carbon nanotubes were grown on the following substrates via chemical vapor deposition (CVD): 5000 Å silicon dioxide (SiO_2), 1300 Å SiO_2, and 40 Å aluminum oxide (Al_2O_3)/5000 Å SiO_2, all on n++ doped silicon substrates. The CNT growths occurred at 875 ºC with a flow of hydrogen, methane, and ethylene gases for 20 min after a 20-min anneal at temperature in argon. Prior to growth, a catalyst was deposited randomly by dipping the substrates in an 80 µg/mL ferric nitrate and isopropanol solution. For the SiO_2 substrates, growth on most of the samples consisted of randomly dispersed SWCNTs 0.5 to 10 microns long. However, there were some interesting exceptions. On a 1300 Å SiO_2 substrate, an anomalously long SWCNT in excess of 75 µm was discovered (figure 1 a and b). While extremely long SWCNTs have been grown by others using a water-assisted "super growth" technique (*2*), we have not attempted that here. On another SiO_2 (3000 Å) substrate there were concentrated meshes of CNTs around the borders of the sample (figure 2a). The latter was probably due to the IPA\catalyst solution beading up around the edges of the substrate when it was dried with nitrogen. There was also some multi-walled CNT growth noted by their larger diameters, 3D conformations, and different charging characteristics, mixed in with the single-walled CNTs (figure 2b).

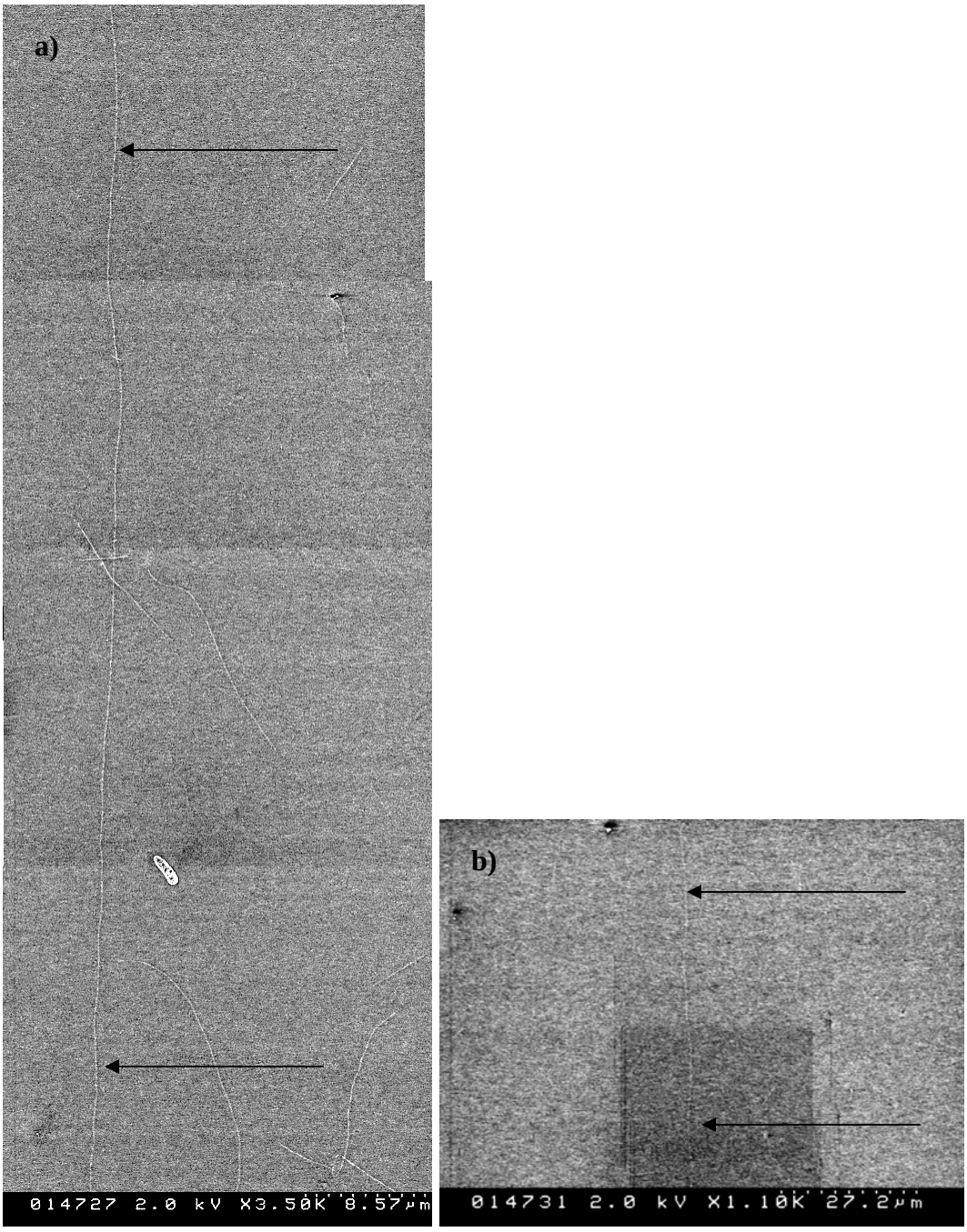


Figure 1. a) Multiple SEM images stiched together of an extremely long SWCNT and b) zoomed out picture of the SWCNT better displaying its actual length.

For the Al_2O_3 sample, barely any CNTs were discovered (figure2c). However there were problems with the oxide layer's lack of charging during the SEM process which we rely on to visualize the CNTs and evaluate growth. Multiple accelerating voltages were tried in an attempt to overcome this problem. A higher magnification image of the oxide showed a nanoparticulate composition (figure 2d). The lack of charging would explain why no CNTs were visible in an SEM image. However, the aluminum oxide layer could also be unsuitable for CNT growth. Few

CNTFETs resulted from the growth on Al_2O_3, likely due to poor growth yields, and when electrically characterized they were metallic in nature. It is unclear if the aluminum oxide is smooth enough to image any CNTs using AFM.

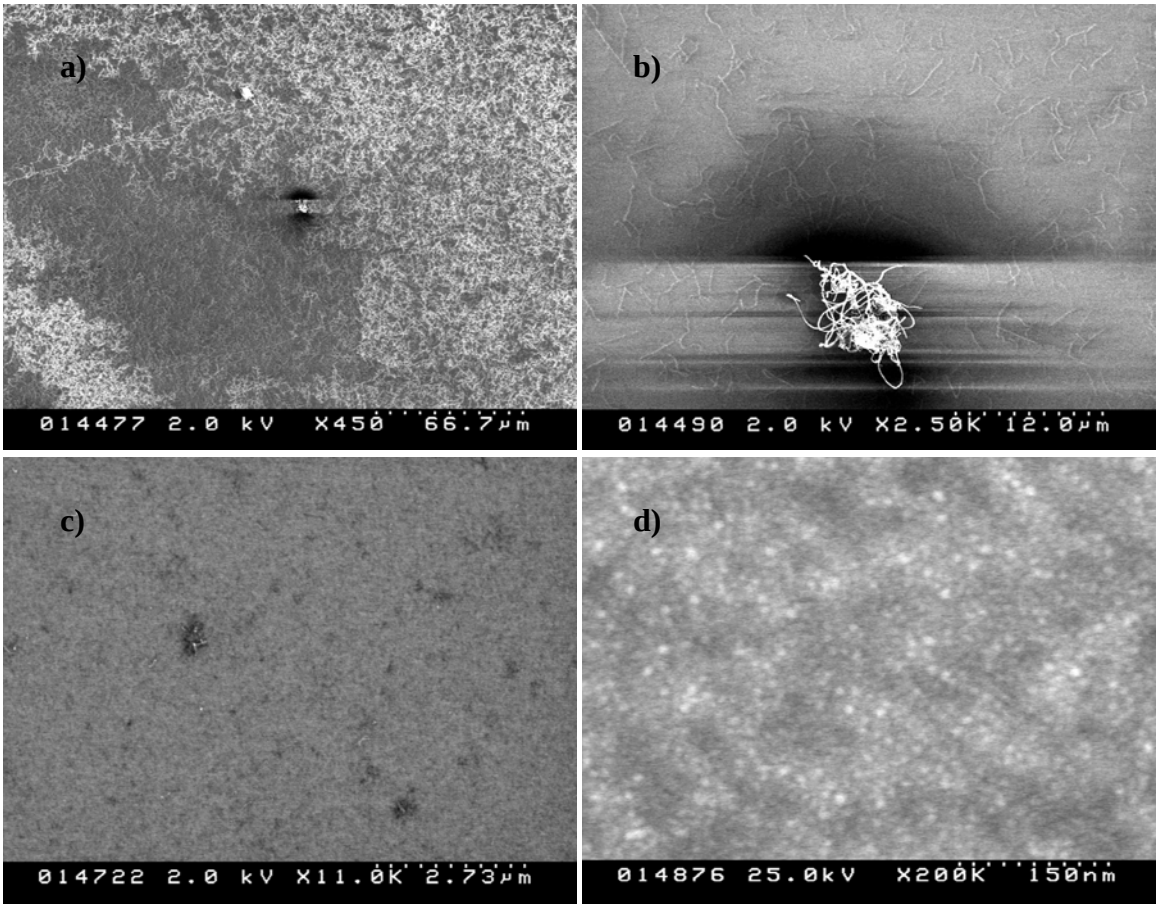


Figure 2. a) Meshes of CNTs on the edge of a substrate, b) multiwalled CNTs mixed in with SWCNTs, c) aluminum oxide substrate with no CNTs visible, and d) high magnification image of nanoparticular aluminum oxide.

2.1.2 CNT Solution Deposition

An alternative method for dispersing CNTs on a substrate is spin-coating samples with a CNT solution. We carried this process out for CNT depositions on 6000 Å SiO_2/n++ doped silicon substrates that were later cut into multiple die. This insured that when we compared different contact metals or suspended versus supported CNTs, CNT dispersal was relatively similar between the two samples so the differences noted in performance could be attributed solely to architecture. Another sample with parylene as the oxide material was spin-coated with CNTs for further comparison.

2.2 Device Processing

2.2.1 Back-gated CNTFETs with Differing Gate Oxides

For this experiment, we processed 5000 Å SiO_2, 1300 Å SiO_2, and 40 Å Al_2O_3/5000 Å SiO_2 on n++ doped silicon substrates using the CVD growth process. We processed two other samples using solution spun CNTs on a 6000 Å SiO_2/n++ doped silicon substrate, as well as a silicon substrate coated in parylene. These samples were made using varying gate dielectric thickness, and materials are used to investigate the effects of the gate dielectric on device noise and hysteresis. For the CVD growth samples, source and drain contacts were patterned using conventional photolithography and metal deposition via e-beam evaporation. Liftoff was performed using a heated bath of Microchem Remover PG. The contacts were 2500 Å gold with a 25 Å chrome adhesion layer. The device substrate is used as a common gate so there was no gate patterning. For the parylene and 6000 Å SiO_2 samples, source and drain contacts were patterned with smaller 2 μm gaps using an image reversal process possible with AZ5214E photoresist. This insured reliable liftoff for fine features because the reverse image process results in a negative sidewall profile in the photoresist. Contacts for these devices were comprised of 2000 Å gold with a 100 Å titanium adhesion layer. Metal layers for both CVD grown and spin-coated CNT samples were deposited via e-beam evaporation.

2.2.2 Back-gated CNTFETs with Differing Contact Metallizations

Different contact metallizations were used to investigate how they affect the contact resistance and $I_{s\,max}$. Again using the image reversal process with AZ 5214E resist, two different die consisting of 6000 Å SiO_2 on n++ doped silicon were patterned for source drain contact metallization. The two die were cut from a single CNT solution deposition so CNT dispersal was relatively similar on both samples. Two metallizations were carried out using e-beam evaporation. The first metallization was 2000 Å gold with a 100 Å chrome adhesion layer and the other was 2000 Å of palladium without an adhesion layer.

2.2.3 Top-gated CNTFETs

Top-gated FETs were fabricated to investigate the gate control and hysteresis that would result from this architecture. Source and drain contacts were patterned consisting of 2500 Å gold on top of a 25 Å chrome adhesion layer. Interdigitated gate electrodes were then patterned in photoresist. 19 Å of aluminum was deposited and allowed to form a native oxide, by exposure to air, of approximately 40 Å. Then a 2500 Å gold layer with a 25 Å chrome adhesion layer was deposited overtop of this. Liftoff was carried out using a heated bath of Microchem Remover PG. After these processing steps, we examined the devices with scanning electron microscopy. We noticed unwanted CNTs that were contributing to the source and drain currents but were not affected by the patterned gates (figure 3a). A mask was made to selectively protect the CNTs that were underneath the aluminum oxide gates with a layer of photoresist (figure 3b). After the resist was patterned, the sample was subjected to an oxygen plasma to remove the unwanted CNTs.

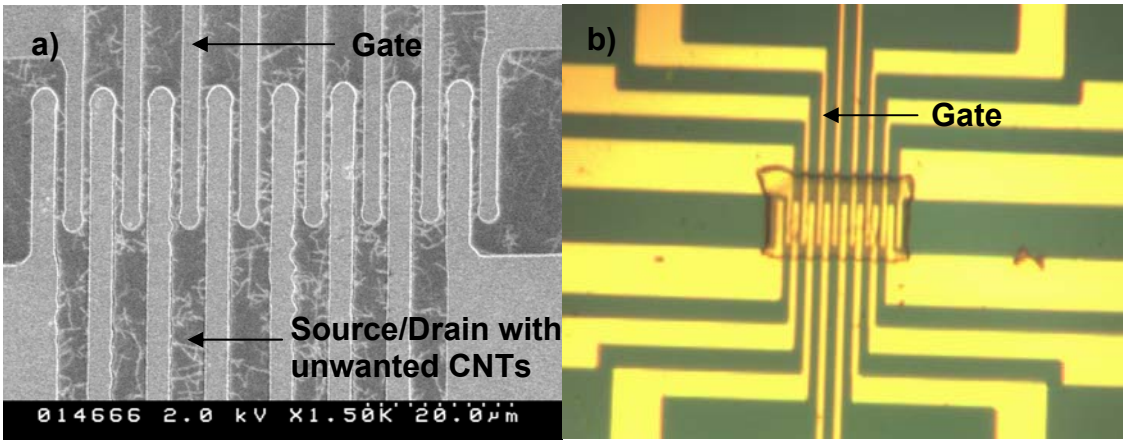


Figure 3. a) Top-gated CNTFETS, with interdigitated source/drain (lower) and gate (upper) electrodes; the source/drain gaps have unwanted CNTs, which are not overlapped by the gate. b) Optical microscope image of patterned resist for the selected removal of CNTs that are outside of the electrode overlap area.

2.2.4 Suspended CNTFETS

In an attempt to remove any gate dielectric effects, we fabricated suspended nanotube FETs. For two samples, metal source and drain electrodes were interdigitated to provide narrower source drain gaps between 1 and 2 µm (figure 4). On one sample, a vapor phase hydrofluoric acid (HF) etch was carried out to remove some of the 5000 Å SiO_2 gate oxide that was underneath the CNTs. This process effectively removed around 2600 Å of SiO_2; however, there is some question as to the degree of the source and drain undercut due to the isotropic nature of this etch. We suspect the CNTs are at least partially suspended above the oxide, but some may have dropped down onto the substrate at the center (see figure 5b). It was difficult to tell the degree of suspension from scanning electron microscopy, as suspended CNTs have no charge difference with a resting oxide, making it difficult to image suspended CNTs. The CNTs, however, were visible due to etch residue left on the CNT by the HF vapors, as shown in figure 4b. Another sample had the same interdigitation of chrome (Cr)/gold (Au) electrodes; however, instead of a vapor phase HF etch, a wet buffered oxide etch (BOE) was carried out. After a 3.5-min BOE etch, the sample was transferred to water to remove any residual HF acid and then transferred to an isopropanol bath to reduce surface tension when drying, increasing the reliability and yield of suspended CNTs. It was allowed to air dry after the isopropanol bath. The etch removed approximately 1400 Å of the SiO_2 oxide layer. The goal of experimenting with this architecture is to verify whether the hysteresis apparent in back-gated CNTFETs is due to charge traps in the gate oxide or due to charge trapping by monolayers of water molecules that surround the CNT (*3*).

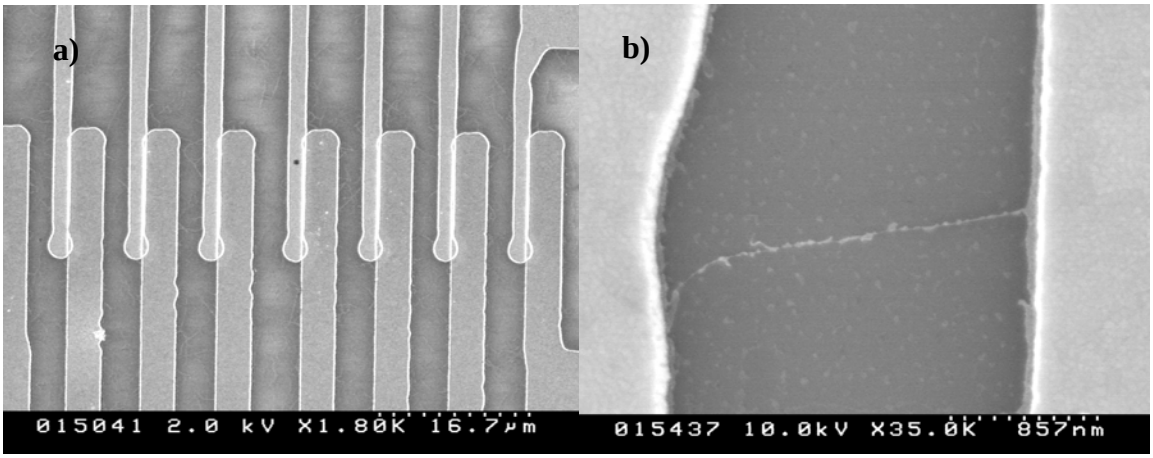


Figure 4. a) Back-gated CNTFET sample before CNT suspension with a gate oxide etch. b) CNT suspended between source and drain contacts after vapor phase HF etch.

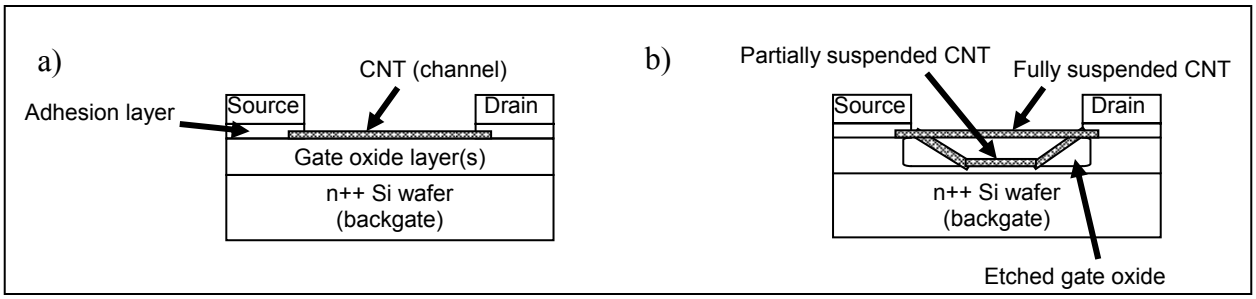


Figure 5. Cross sectional drawings of: a) a typical back-gated CNTFET, and b) a suspended CNTFET with fully and partially suspended tubes shown.

3. Results and Discussion

All devices were characterized with a Keithley 4200-SCS semiconductor characterization tool with up to three independent probes. The CNTFET source-drain bias applied for all gate voltage sweeps was 250 mV except where noted. The variations in the CNTFET architectures investigated here were found to affect many aspects of the devices, such as the $I_{s\ max}$, noise, and hysteresis.

3.1 Maximum and Minimum Source Current

The main difference we noted between samples with different contact metallizations was the maximum on-current of the transistor ($I_{s\ max}$). Again, one sample had 2000 Å gold with a 100 Å chrome adhesion layer, and the other had 2000 Å of palladium contacts. The samples with

palladium source-drain contacts appear to have much lower contact resistance than any of the devices with a chrome adhesion layer. The Pd contact samples had higher $I_{s\,max}$ when devices with each metallization were made from pieces of the same CNT coated Si die (identical tube densities). This is due to the differing work functions of these metals (*4, 5*). The junction between the CNT and the contact metal is known to introduce a Schottky barrier, based on the work function difference between the metal and the CNT (*6, 7*). CNTs have been shown to have a work function somewhere around 4.9 eV (*8*). Chrome has a work function of roughly 4.5 eV, and palladium has a work function of 5.1 eV. The closer the work functions of the two materials are, the weaker the resulting Schottky barrier is. Therefore, palladium has less of a barrier height and a lower contact resistance, making it ideal for higher current CNTFETs.

Annealing, while not affecting the device architecture, is also found to significantly affect $I_{s\,max}$. Initial testing of a high current palladium device before annealing yielded poor results with $I_{s\,max}$ ≈ 700 nA (figure 6a). After a 15 min hotplate bake at 250 ºC, $I_{s\,max}$ ≈ 20 μA (figure 6b). This represents a large drop in contact resistance to about 3.5 % of the initial value. Therefore, annealing, as well as the contact metallization, can affect the contact resistances/$I_{s\,max}$.

$I_{s\,min}$ is another issue completely, and it is important as it relates to the on/off ratio of the device. Since the CNT solution used to spin on the CNTs was a mixture of metallic and semiconducting tubes, the resulting transistors would not turn off completely, as shown in figure 6. Because of the metallic nature of some of the spun-on tubes, $I_{s\,min}$ ≈ 10 μA. However, it is possible to transform this mixed metallic-semiconducting CNTFET to a completely semiconducting CNTFET through a process that selectively burns off metallic carbon nanotubes shown in figure 7 (*9*). At high positive gate voltages (e.g., +20 V), current only flows through the metallic tubes because the gate field has the semiconducting CNTs “turned off”. Therefore, multiple source-drain voltage ramps up to 18 V and back to 0 V were performed while keeping the gate at a bias of +20 V (figure 7a). Sudden drops in current can be attributed to the burning off of metallic carbon nanotubes. After this process, the final CNTFET has an $I_{s\,max}$ ≈ 1μA and a $I_{s\,min}$ ≈ 5 nA, representing an improvement of the on/off ratio from 2 to 200 (figure 7b). This process provides a reliable way to create all semiconducting CNTFETs with reasonable on/off ratios.

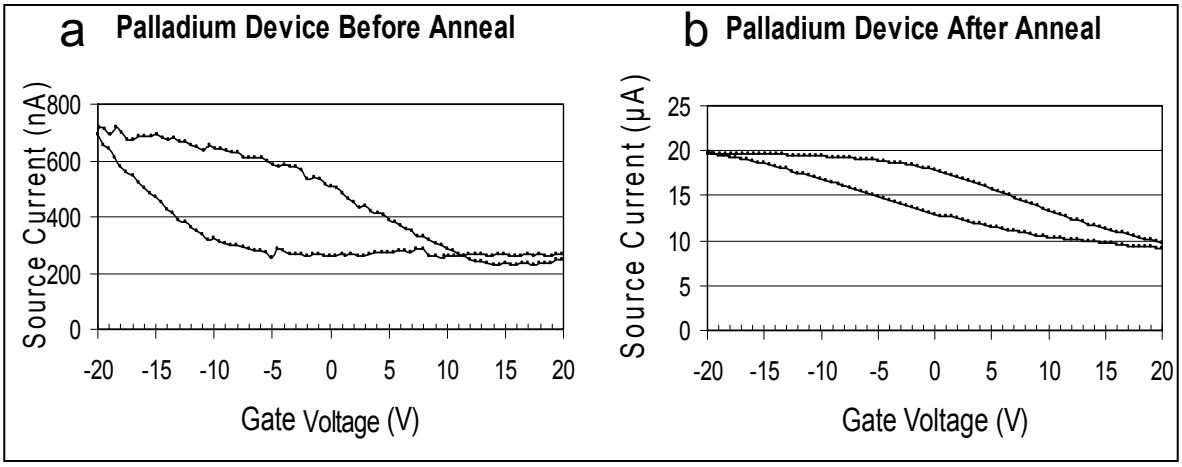


Figure 6. CNTFET after palladium deposition a) before anneal and b) after anneal.

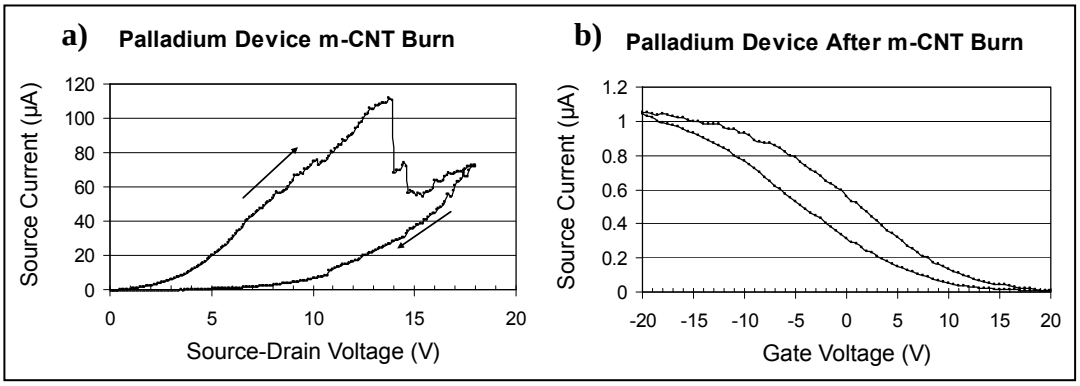


Figure 7. a) Metallic CNT burnoff process for the palladium CNTFET shown in figure 6. b) Resulting CNTFET after all conditioning steps.

3.2 Noise

We investigated devices with different oxides for their noise characteristics. Two back-gated samples were processed to compare the effects the gate oxide type has on device noise. One sample had a 10 μm parylene dielectric layer on an insulating Si wafer (and, therefore, no gate control), and the other had a standard 0.5 μm SiO_2 dielectric. Both samples were subjected to a time domain test where the source-drain voltage (V_{sd}) was held constant at a direct current (DC) bias of 0.5, 1, or 2 V, and V_g was held constant at 0 V. The resulting signal could be modeled as a constant DC with some type of white noise. This noise may have contributions from both the intrinsic nature of the CNT, as well as the oxide. Signal-to-noise ratios (SNR) were calculated based on these measurements for several different devices on both the parylene and SiO_2 samples.

The SNR of a parylene device was measured before and after annealing. These results confirmed earlier suspicions about the positive effects of contact annealing after the metallization step. The anneal was simply a 15 min bake on a 250 ºC hotplate in open air. This step alone improved the SNR of the device by 7.0 dB (figure 8a). This is either due to driving off any chemical contamination left on the tube after processing or reducing the contact resistance at the metal-CNT junction. Another important finding from the analysis of the noise data was the difference between the SNRs of the parylene and SiO_2 devices. The average SNR for all parylene devices tested after annealing them was 13.0 dB. The SiO_2 samples were subjected to the same anneal and the average SNR recorded was 17.9 dB (figure 8b). This supports other research showing that the 1/f noise noted in CNTFETs is critically affected by the oxide (*10, 11*). This noise is due to charge traps in the oxide. The trapping and detrapping of carriers in the oxide causes minor fluctuations in the current noted in these CNTFETs (*6, 7*).

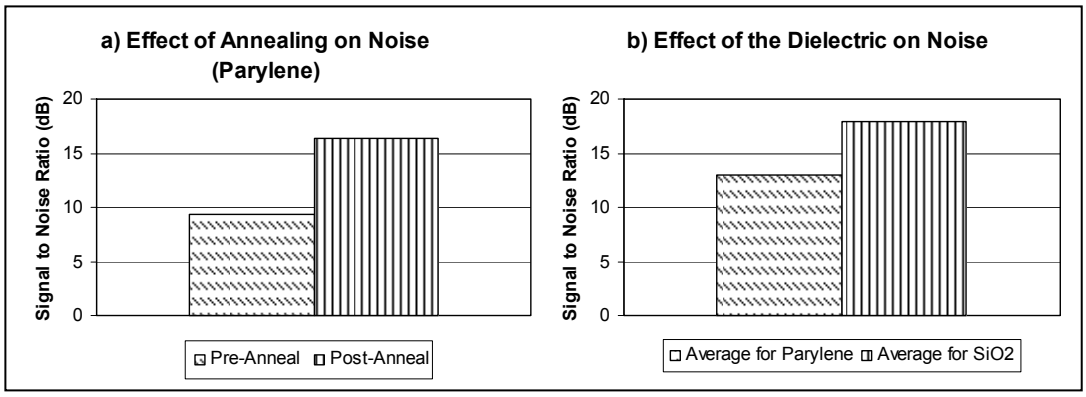


Figure 8. a) Comparison showing SNR increase after an anneal of the CNTFET. b) Comparison showing SNR higher on average for SiO_2 devices than for parylene devices.

3.3 Hysteresis

3.3.1 Back-gated CNTFETs with Differing Gate Oxides

Various approaches have been taken to try to affect device hysteresis. Different oxide thicknesses, back- versus top-gated devices, and suspended CNT devices were investigated.

For 5000 Å SiO_2 back-gated CNTFETs, there exists a considerable amount of hysteresis. However, in testing these devices, hysteresis can be minimized by narrowing the gate voltage (V_g) range from $-20 \leq V_g \leq 20$ to $-10 \leq V_g \leq 10$ (figure 9a). This does not by itself distinguish whether the hysteresis is caused by charge traps in the oxide or from H_2O molecule dipoles on the CNT surface.

The thinner oxide (1300 Å SiO_2) back-gated devices showed a couple of variations. Most of the devices had lower currents (figure 9b). This is most likely due to lower CNT growth density on this sample. (The yield of devices with CNTs bridging the source drain contacts was very low when examined by SEM.) Most other properties, such as hysteresis and sub-threshold slope,

were comparable to 5000 Å SiO_2 back-gated devices. It should be noted that the gate voltage range was decreased to produce a gate field similar to the 5000 Å gate devices in order to facilitate a comparison of the device performances.

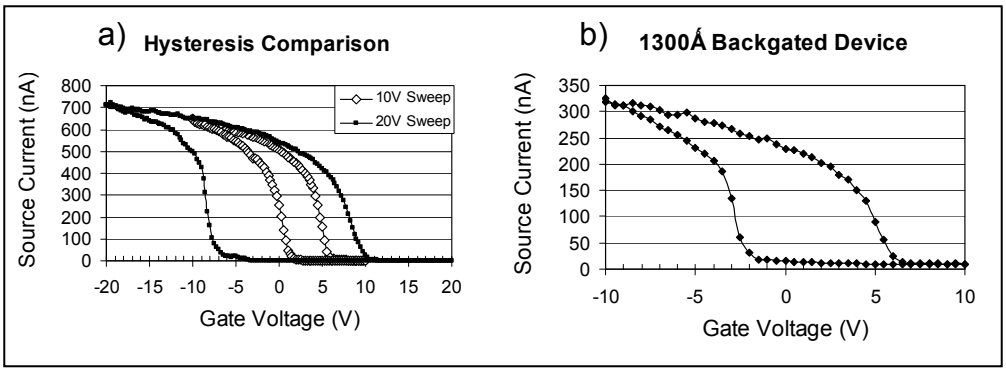


Figure 9. a) Comparison showing hysteresis change with reduced gate voltage ranges. b) Example of a single tube device grown on 1300 Å SiO_2.

3.3.2 Top-gated CNTFETs

We took many considerations before testing the Al_2O_3 top-gated devices. The gate oxide layer is approximately 40 Å thick, so the gate voltage range needed to be scaled down considerably. If too much gate voltage is applied, then breakdown of the thin gate oxide could easily occur. The gate voltage range was scaled down to -700 mV $\leq V_g \leq$ 700 mV with V_{sd} decreased to 50 mV. Final source/drain current compliance was set to 10 nA. The results showed almost no visible signs of hysteresis (figure 10). When the aluminum layer was deposited (to eventually form a native oxide of Al_2O_3), it was done via electron beam evaporation. During the vacuum pump-down of the evaporator chamber, most of the residual water molecules were removed from the exposed CNTs. The deposited top-gates then, in effect, passivated the CNTs from further exposure to ambient conditions. The photoresist layer used for selective plasma ashing also served as a passivation layer. This appears to show that reorientation of water molecule dipoles surrounding the carbon nanotube are responsible for most of the hysteresis appearing in our CNTFETs. About 1 nA of gate leakage, resulting from oxide breakdown, was noticed in this device after a gate bias of –400 mV. The device has an $I_{s\,max} \approx 4.1$ nA at a V_g of 400 mV.

3.3.3 Suspended CNTFETs

The samples with suspended CNTs were characterized before and after their respective gate oxide etches. Changes to device hysteresis were noticed for two gate voltage ranges, $-20 \leq V_g \leq 20$ and $-10 \leq V_g \leq 10$, for the samples that were subjected to a vapor phase HF etch (figure 11). In both cases, an increase in hysteresis was noted. Sub-threshold slope was relatively unchanged; however, there was some shift in threshold voltage. There was also a decrease in $I_{s\,max}$, which was due to the fact that not all of the tubes originally bridging the source drain gap were intact after the suspension process. For the samples suspended using a buffered oxide etch, fewer

devices survived when compared to the vapor phase HF sample; however, an increase in hysteresis was noticed in the devices that remained. For these samples, more CNT surface area was exposed to open air than when they were lying directly on an oxide. A consequence of this is more nanotube exposure to water molecules and contaminants in ambient air, and less of the tubes are lying on the gate oxide. Therefore, hysteresis in these devices is thought to be most likely caused by water molecule dipoles (*3*) or other environmental contaminants than by charge traps in the gate oxide layers (*12*).

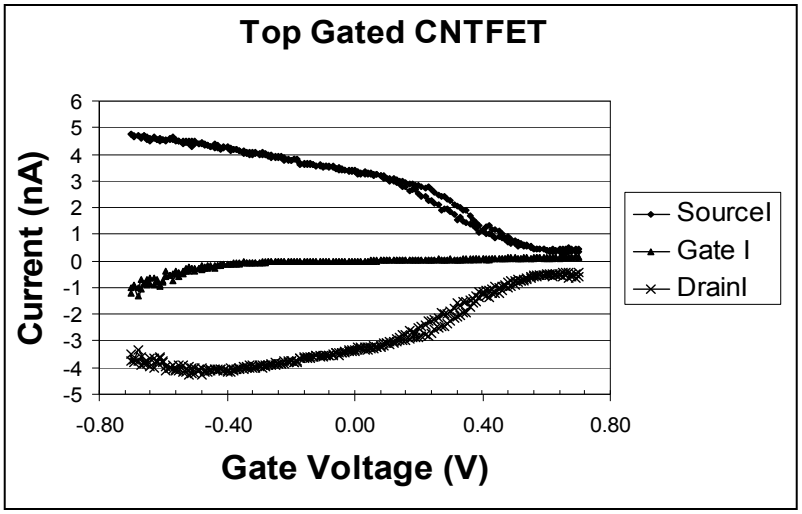


Figure 10. Source, drain, and gate characteristics for a gate voltage sweep of a top-gated CNTFET.

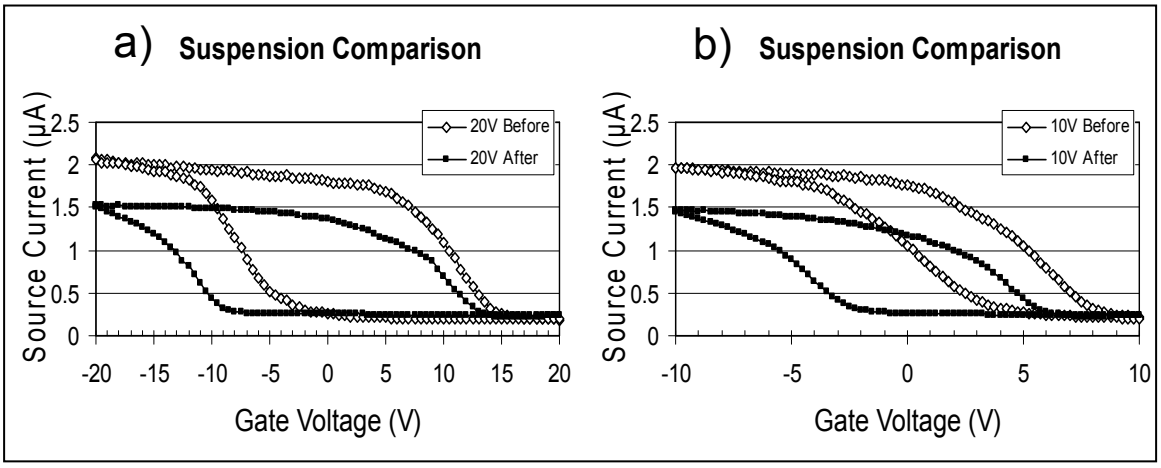


Figure 11. a) Comparison before and after vapor phase HF etch on suspension sample for a ±20 V gate sweep. b) Comparison for a ±10 V gate sweep.

4. Summary and Conclusions

Understanding the differing methods and materials that can be used for producing CNT based electronic components is extremely important. An informed use of materials and architectures will unleash the potential of CNTFETs for a wide array of future electronic applications. CNTFET device architecture has been shown to affect the properties of CNTFETs, which includes the $I_{s\ max}$, noise, and hysteresis. Other properties, such as the metallic or semiconducting nature of these devices, determined by tube chirality, as well as sub-threshold slope, are not greatly affected by device architectures (*1, 4*). We have shown that an appropriate choice of contact metallization, annealing conditions, and CNT density can all increase $I_{s\ max}$. While $I_{s\ min}$ cannot be similarly controlled due to the mixture of semiconducting and metallic tubes as-grown or as-deposited, good on/off ratios can be achieved by burning off the metallic tubes. Annealing and the choice of gate dielectric were found to affect the device noise and the SNR. Hysteresis was shown to be a property of the CNTFET that can be, for the most part, eliminated with appropriate device geometry, such as a top-gate architecture that provides environmental passivation. This will be advantageous for electronic applications, while greater hysteresis due to environmental exposure may indicate a device architecture that is well suited to chemical sensing applications. While a single device architecture will not be optimum for all applications, there are a number of variables that can be tuned to optimize these devices for a given application.

5. References

1. Anantram, M. P.; Leonard, F. Physics of Carbon Nanotube Electronic Devices. *Reports on Progress in Physic* **2006**, *69*, 507–561.

2. Patole, S. P.; Alegaonkar, P. S.; Lee, H.-C.; Yoo, J.-B. Optimization of Water Assisted Chemical Vapor Deposition Parameters for Super Growth of Carbon Nanotubes. *Carbon* **2008**, *46*, 1987–1993.

3. Kim, W.; Javey, A.; Vermesh, O.; Wang, Q.; Li, Y., Dai, H. Hysteresis Caused by Water Molecules in Carbon Nanotube Field-Effect Transistors. *Nano Letters* **2003**, *3–2*, 193–198.

4. Chen, Z.; Appenzeller, J.; Knoch, J.; Lin, Y.-M.; Avouris, P. The Role of Metal-nanotube Contact in the Performance of Carbon Nanotube Field-effect Transistors. *Nano Letters* **2005**, *5*, 1497–1502.

5. Javey, A.; Guo, J.; Farmer, D. B.; Wang, Q.; Wang, D.; Gordon, R. G.; Lundstrom, M.; Dai, H. Carbon Nanotube Field-Effect Transistors with Integrated Ohmic Contacts and High-k Gate Dielectrics. *Nano Letters* **2004**, *4–3*, 447–450.

6. Dai, H.; Javey, A.; Pop, E.; Mann, D.; Lu, Y. Electrical Transport Properties and Field-Effect Transistors of Carbon Nanotubes. *NANO: Brief Reports and Reviews* **2006**, *1–1*, 1–8.

7. Luquette, B. E.; Nichols, B. M. *Fabrication and Characterization of Schottky Diodes using Single Wall Carbon Nanotubes*; ARL-TR-4534; U.S. Army Research Laboratory: Adelphi, MD, August 2008.

8. Yang, M. H.; Teo, K.B.K.; Milne, W. I.; Hasko, D. G. Carbon Nanotube Schottky Diode and Directionally Dependent Feld-effect Transistor Using Asymmetrical Contacts. *Applied Physics Letters* **2005**, *87*, 253116.

9. Seidel, R.; Graham, A. P.; Unger, E. U.; Duesberg, G. S.; Liebau, M.; Steinhoegl, W.; Kreupl, F.; Hoenlein, W.; Pompe, W. High-current Nanotube Transistors. *Nano Letters* **2004**, *4*, 831–834.

10. Lin, Y.; Tsang, J. C.; Freitag, M.; Avouris, Ph. Avouris. Impact of Oxide Substrate on Electrical and Optical Properties of Carbon Nanotube Devices. *Nanotechnology* **2007**, *18*, 295202.

11. Appenzeller, J.; Lin, Y.; Knoch, J.; Chen, Z.; Avouris, Ph. Avouris. 1/f Noise in Carbon Nanotube Devices-On the Impact of Contact and Device Geometry. *IEEE Transactions on Nanotechnology* **2007**, *6–3*, 368–373.

12. Fuhrer, M. S.; Kim, B. M.; Durkop, T.; Brintlinger, T. High-mobility Nanotube Transistor Memory. *Nano Letters* **2002**, *2*, 755.

List of Symbols, Acronyms, and Abbreviations

Al_2O_3	aluminum oxide
Au	gold
BOE	buffered oxide etch
CNT	carbon nanotube
CNTFET	carbon nanotube field-effect transistor
Cr	chromium
CVD	chemical vapor deposition
DC	direct current
HF	hydrofluoric acid
SiO_2	silicon oxide
SNR	signal-to-noise ratio
SWCNT	single-walled carbon nanotube field-effect transistor

No. of Copies	Organization
1	ADMNSTR
ELECT	DEFNS TECHL INFO CTR ATTN DTIC OCP 8725 JOHN J KINGMAN RD STE 0944 FT BELVOIR VA 22060-6218
1	DARPA ATTN IXO S WELBY 3701 N FAIRFAX DR ARLINGTON VA 22203-1714
1 CD	OFC OF THE SECY OF DEFNS ATTN ODDRE (R&AT) THE PENTAGON WASHINGTON DC 20301-3080
1	US ARMY RSRCH DEV & ENGRG CMND ARMAMENT RSRCH DEV/ENGRG CTR ARMAMENT ENGRG & TECHNLGY CTR ATTN AMSRD AAR AEF T J MATTS BLDG 305 ABERDEEN PROVING GROUND MD 21005-5001
1	PM TIMS, PROFILER (MMS-P) AN/TMQ-52 ATTN B GRIFFIES BUILDING 563 FT MONMOUTH NJ 07703
1	US ARMY INFO SYS ENGRG CMND ATTN AMSEL IE TD A RIVERA FT HUACHUCA AZ 85613-5300
1	COMMANDER US ARMY RDECOM ATTN AMSRD AMR W C MCCORKLE 5400 FOWLER RD REDSTONE ARSENAL AL 35898-5000
1	US GOVERNMENT PRINT OFF DEPOSITORY RECEIVING SECTION ATTN MAIL STOP IDAD J TATE 732 NORTH CAPITOL ST NW WASHINGTON DC 20402
1	US ARMY RSRCH LAB ATTN RDRL CIM G T LANDFRIED BLDG 4600 ABERDEEN PROVING GROUND MD 21005-5066
15 HCs 1 PDF	US ARMY RSRCH LAB ATTN RDRL CIM P TECHL PUB ATTN RDRL CIM L TECHL LIB ATTN RDRL SER L B PIEKARSKI ATTN RDRL SER L M DUBEY ATTN RDRL SER L M ERVIN (1 PDF, 10 HCs) ATTN IMNE ALC HRR MAIL & RECORDS MGMT ADELPHI MD 20783-1197

TOTAL:25 (22 HCs, 1 CD, 1 PDF, 1 ELECT)