NASA CASE NO. LAR 13950-1

PRINT FIG. 1

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LaRC

NASA Case No. LAR 13950

AWARDS ABSTRACT

PRINTER PORT INTERFACE

A number of methods are available for interfacing to personal computers (PC). One method is to interface directly to the PC's internal bus. This method requires a special card to be placed inside the PC. Another method is to interface through the RS232 serial port. The data transfer rate using this method is very slow and the data must be converted from serial to parallel. Various other methods exist which require internal cards and/or special circuitry within the PC.

A novel interface device has been designed which converts a standard printer port into a general purpose bus so that a number of external devices or microprocessor peripheral integrated circuits may be connected to a personal computer via the printer port on the personal computer. The interface device connects the external device to the personal computer and in *write* mode, receives data from the personal computer, signals the external device to accept the information, and sends the data to the external device and in *read* mode signals the external device to provide data, receives data from the external device and sends the data in amounts which do not exceed the input limits of the printer port to the personal computer.

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PRINTER PORT INTERFACE

Origin of the Invention

The invention described herein was made by employees of the United States Government and may be used by and for the Government for governmental purposes without the payment of any royalties thereon or therefor.

Technical Field of the Invention

The present invention relates generally to interface devices, and more particularly to an interface device which is connected to a printer port on a personal computer.

Background of the Invention

A number of methods are available for interfacing to personal computers (PC). One method is to interface directly to the PC's internal bus. This method requires a special card to be placed inside the PC. Another method is to interface through the RS232 serial port. The data transfer rate using this method is very slow and the data must be converted from serial to parallel. Various other methods exist which require internal cards and/or special circuitry within the PC.

It is accordingly an object of the present invention to provide an interface which converts the printer port on a personal computer to a general purpose bus.

It is another object of the present invention to provide an interface which is capable of causing the printer port on a personal computer to emulate a simple 8 bit microprocessor.

It is another object of the present invention to provide an interface which is capable of connecting many different devices, including microprocessor peripheral integrated circuits, to a personal computer.

It is another object of the present invention to provide an interface which does not require additional cards to be installed inside the personal computer.

It is another object of the present invention to provide bidirectional data transfer.

It is yet another object of the present invention to accomplish the foregoing objects in a simple manner.

Additional objects and advantages of the present invention are apparent from the drawings and specification which follow.

Summary of the Invention

According to the present invention, the foregoing and additional objects are obtained by providing a device which converts a standard printer port into a general purpose bus so that a number of external devices or microprocessor peripheral integrated circuits may be connected to a personal computer via the printer port on the personal computer. The interface device connects the external device to the personal computer and in *write* mode, receives data from the personal computer, signals the external device to accept the information, and sends the data to the external device and in *read* mode signals the external device to provide data, receives data from the external device and sends the data in amounts which do not exceed the input limits of the printer port to the personal computer. The *write* mode may be accomplished by having the interface device receive address, data and control information from the personal computer, latch the address and data on proper output lines, and signal the external device to accept the information. The *read* mode may be accomplished by having the

interface device receive address and control information from the personal computer, signal the external device to provide data, receive data from the external device and send the data to the personal computer in amounts which do not exceed the input limits of the printer port.

Brief Description of the Drawings

Fig. 1 is a block diagram showing an embodiment of the present invention.

Detailed Description of the Invention

Fig. 1 shows one embodiment of the invention. In this embodiment the PC's printer port provides PC DATA consisting of the eight output terminals 1_1-1_8, PC CONTROL OUT consisting of the four output terminals 2_1-2_4, and PC CONTROL IN consisting of the five input terminals 3_1-3_5. These signals are sent and received by the printer port under control of software running on the PC.

The selected embodiment of the invention consists of six components the CONTROL LATCH, the DECODER, the SELECTOR, the HIGH ADDR LATCH, the LOW ADDR LATCH, and the DATA LATCH. A device suitable for use as the CONTROL LATCH, HIGH ADDR LATCH, LOW ADDR LATCH, and DATA LATCH is a 74LS374. A device suitable for the DECODER is a 74LS138, and a device suitable for the SELECTOR is a 74LS244. These devices are available from various semiconductor manufacturers. The CONTROL LATCH 4 has eight data input terminals connected to PC DATA terminals 1_1-1_8, and eight data output terminals 5_1-5_8. The data output terminals are tri-stated unless the OE terminal 6 is "0". The CLK terminal 7 is connected to PC CONTROL OUT terminal 2_3. A "0" to "1" transition on the CLK terminal 7 causes the value of 1_1-1_8 to be

transferred to the output terminals 5_1-5_8. The DECODER 8 has eight output terminals 9_1-9_8. When the EN input terminal 10 is a "0" then one of the outputs 9_1-9_8 goes to "0". The particular output is determined by the value applied to input terminals 11_1-11_3. The SELECTOR 12 has eight input terminals 13_1-13_8. If input terminal 14_1 is a "0" then the value on input terminals 13_1-13_4 is gated to the four output terminals 15_1-15_4. If input terminal 14_2 is a "0" then the value on input terminals 13_5-13_8 is gated to the four output terminals 15_1-15_4. The DATA LATCH 16, the HIGH ADDR LATCH 17, and the LOW ADDR LATCH 18 are identical to the CONTROL LATCH 4. The eight data input terminals of latches 16, 17, and 18 are connected to PC DATA 1_1-1_8. When the OE input 19 of DATA LATCH 16 is "0", a "0" to "1" transition on CLK input 20 will cause the value of 1_1-1_8 to be transferred to the output terminals 21_1-21_8. When the OE input 22 of HIGH ADDR 17 is "0", a "0" to "1" transition on CLK input 23 will cause the value of 1_1-1_8 to be transferred to the output terminals 24_1-24_8. When the OE input 25 of LOW ADDR LATCH 18 is "0", a "0" to "1" transition on CLK input 26 will cause the value of 1_1-1_8 to be transferred to the output terminals 27_1-27_8. PC DATA TERMINAL 1_1 is connected directly to PC CONTROL IN terminal 3_5. This connection is used to determine if the selected embodiment is present and to identify the printer port to which it is connected.

An external device is connected to the selected embodiment using the bi-directional data terminals D_0-D_7, the address terminals A_0-A_{15}, read control terminal /RD, write control terminal /WR, and various SPARE terminals with uses that are dependent upon the particular external device. The bi-directional data terminals D_0-D_7 are connected to lines 13_1-13_8 of SELECTOR 12 and lines 21_1-21_8 of DATA LATCH 16. The address terminals A_8-A_{15} are connected to lines 24_1-24_8 HIGH ADDR LATCH 17 and address terminals A_0-A_7 are connected to lines 27_1-27_8 of LOW ADDR LATCH 18. The read control terminal /RD is connected to line 5_7 of CONTROL LATCH 4, and the write control terminal /WR is connected to line

5_8 of CONTROL LATCH 4. In this embodiment the PC CONTROL OUT terminal 2_1, line 5_6 of CONTROL LATCH 4, and lines 9_6-9_8 of DECODER 8 are all SPARE terminals with uses that can be defined to accommodate a particular application.

The two modes of operation for the invention are *read* and *write*. The function of the embodiment of the invention during the write operation is to transform information received from the PC's printer port to sixteen bits of address, eight bits of data, and a write pulse which will be accepted by an external device. The write operation consists of 23 steps. Steps 1-6 describe the output of the low eight bits of a sixteen bit address. Steps 7-12 describe the output of the high 8 bits of the address, and steps 13-23 describes the output of the eight bits of data.

Step 1: The PC outputs a value of "1" to 1_1, and a value of "0" to 1_2 and 1_3. This will be used to force 9_2 to "0" prior to clocking LOW ADDR LATCH 18.

Step 2: The PC outputs a value of "1" to 2_2. This disables the DECODER 8 and causes its outputs 9_1-9_8 to assume a value of "1". At the same time the PC also outputs a value of "0" to 2_3. This insures that the CONTROL LATCH 4 clock input 7 is a "0".

Step 3: The PC outputs a value of "1" to 2_3 and a value of "0" to 2_4. This clocks and enables the CONTROL LATCH 4 and causes the value of "001" that was output to 1_3, 1_2, and 1_1 in Step 1 above to be transferred to the CONTROL LATCH outputs 5_1-5_3, which are connected to DECODER 8 inputs 11_1-11_3.

Step 4: The PC outputs the low byte of a 16 bit address to 1_1-1_8.

Step 5: The PC outputs a "0" to 2_2. This enables the DECODER 8. The value "001" that was transferred to the DECODER inputs 11_1-11_3 in Step 3 above causes the DECODER output 9_2 and thus the LOW ADDR LATCH clock input 26 to assume a value of "0".

Step 6: The PC outputs a value of "1" to DECODER enable pin 2_2. This disables the DECODER so that the DECODER output 9_2 changes from "0"

to "1". Since 9_2 is connected to LOW ADDR LATCH clock input 26, the low byte of address that was placed on 1_1-1_8 in Step 4 is latched to LOW ADDRESS LATCH outputs 27_1-27_8.

Step 7: The PC outputs a value of "0" to PC DATA terminals 1_1-1_3. This will be used force 9_1 to "0" prior to clocking HIGH ADDR LATCH 17.

Step 8: The PC outputs a value of "1" to 2_2. This disables the DECODER 8 and causes its outputs 9_1-9_8 to assume a value of "1". At the same time the PC also outputs a value of "0" to 2_3. This insures that the CONTROL LATCH 4 clock input 7 is a "0".

Step 9: The PC outputs a value of "1" to 2_3 and a value of "0" to 2_4. This clocks and enables the CONTROL LATCH 4 and causes the value of "000" that was output to 1_3, 1_2, and 1_1 in Step 7 above to be transferred to the CONTROL LATCH outputs 5_1-5_3 which are connected to DECODER inputs 11_1-11_3.

Step 10: The PC outputs the high byte of a 16 bit address to 1_1-1_8.

Step 11: The PC outputs a "0" to 2_2. This enables the DECODER 8. The value "000" that was transferred to the DECODER inputs 11_1-11_3 in Step 9 above causes the DECODER output 9_1 and thus the HIGH ADDR LATCH clock input 23 to assume a value of "0".

Step 12: The PC outputs a value of "1" to DECODER enable pin 2_2. This disables the DECODER 8 so that the DECODER output 9_1 changes from "0" to "1". Since the DECODER output 9_1 is connected to HIGH ADDR LATCH clock input 23, the high byte of address that was placed on 1_1-1_8 in Step 10 is latched to HIGH ADDRESS LATCH outputs 24_1-24_8.

Step 13: The PC outputs a value of "0" to 1_3-1_5, a value of "1" to 1_2, and a value of "0" to 1_1.

Step 14: The PC outputs a value of "1" to 2_2. This disables the DECODER 8 and causes its outputs 9_1-9_8 to assume a value of "1". At the same time the PC also outputs a value of "0" to 2_3. This insures that the CONTROL LATCH 4 clock input 7 is a "0".

Step 15: The PC outputs a value of "1" to 2_3 and a value of "0" to 2_4. This clocks and enables the CONTROL LATCH 4 and causes the value of "00010" that was output to 1_5- 1_1 in Step 13 above to be transferred to the CONTROL LATCH outputs 5_5-5_1.

Step 16: The PC outputs the data to terminals 1_1-1_8.

Step 17: The PC outputs a "0" to 2_2. The value of "010" that was transferred to the DECODER inputs 11_1-11_3 in Step 15 above causes the DECODER output 9_3 and thus the DATA LATCH clock input 20 to assume a value of "0".

Step 18: The PC outputs a value of "1" to DECODER enable pin 2_2. This disables the DECODER so that the DECODER output 9_3 changes from "0" to "1". Since 9_3 is connected to DATA LATCH clock input 20 the data byte that was placed on 1_1-1_8 in Step 16 is latched to DATA LATCH outputs 21_1-21_8.

Step 19: The PC outputs a value of "0" to 1_8. This will be used to activate the /WR terminal by forcing it to "0".

Step 20: The PC outputs a value of "1" to 2_2. This disables the DECODER 8 and causes its outputs 9_1-9_8 to assume a value of "1". At the same time the PC also outputs a value of "0" to 2_3. This insures that the CONTROL LATCH 4 clock input 7 is a "0".

Step 21: The PC outputs a value of "1" to 2_3 and a value of "0" to 2_4. This clocks and enables the CONTROL LATCH 4 and causes the value of "0" that was output to 1_8 in Step 19 above to be transferred to the CONTROL LATCH output 5_8 which is connected to the /WR terminal.

Step 22: The PC outputs a value of "1" to 1_8, 1_5, and 1_4. This will be used to raise /WR to a "1" and to disable the output of latches 16, 17, and 18.

Step 21: The PC outputs a value of "1" to 2_2. This disables the DECODER 8 and causes its outputs 9_1-9_8 to assume a value of "1". At the same time the PC also outputs a value of "0" to 2_3. This insures that the CONTROL LATCH 4 clock input 7 is a "0".

Step 23: The PC outputs a value of "1" to 2_3 and a value of "0" to 2_4. This clocks and enables the CONTROL LATCH 4 and causes the value of "1" that was output to 1_4, 1_5, and 1_8 in Step 22 above to be transferred to the CONTROL LATCH outputs 5_4, 5_5, and 5_8. The "1" on 5_4 disables the LOW ADDR LATCH 18 and HIGH ADDR LATCH 17. The "1" on 5_5 disables the DATA LATCH 16. The "1" on 5_8 causes the /WR terminal to return to a value of "1".

The *read* process consists of fourteen steps. The output of the low eight bits and high eight bit of the address is described in step 1. The procedure for reading eight bits of data four bits at a time is described in steps 2-14.

Step 1: The PC outputs a 16 bit address using the same procedure outlined in Steps 1-12 of the *write* process described above.

Step 2: The PC outputs a value of "1" on terminals 1_5 and 1_3, and outputs a value of "0" on terminals 1_1, 1_2, 1_4, and 1_7. The value of "100" on 1_3-1_1 will be used to select D4-D7, which are connected to SELECTOR inputs 13_5-13_8. The "0" on 1_4 will be used to enable the HIGH ADDRESS LATCH outputs 24_1-24_8 and LOW ADDRESS LATCH outputs 27_1-27_8. The "1" on 1_5 will be used to disable DATA LATCH outputs 21_1-21_8. The "0" on 1_7 will be used to activate the /RD terminal.

Step 3: The PC outputs a value of "1" to 2_2. This disables the DECODER 8 and causes its outputs 9_1-9_8 to assume a value of "1". At the same time the PC also outputs a value of "0" to 2_3. This insures that the CONTROL LATCH 4 clock input 7 is a "0".

Step 4: The PC outputs a value of "1" to 2_3 and a value of "0" to 2_4. This clocks and enables the CONTROL LATCH 4 and causes the value that was output in Step 2 above to be transferred to the corresponding outputs of CONTROL LATCH 4.

Step 5: The PC outputs a value of "0" to 2_2 which enables the DECODER 8. The value of "100" that was transferred to DECODER inputs 11_3-11_1 in Step

4 above causes the DECODER output 9_5 and thus SELECTOR input 14_2 to assume a value of "0". This causes the D4-D7 values on SELECTOR inputs 13_5-13_8 to be gated to SELECTOR outputs 15_1-15_4 and thus PC CONTROL IN terminals 3_1-3_4.

Step 6: The PC reads the data values D4-D7 on PC CONTROL IN terminals 3_1-3_4.

Step 7: The PC outputs a value of "0" on terminal 1_3, and outputs a value of "1" on terminals 1_1, and 1_2. The value of "011" on 1_3-1_1 will be used to select D0-D3, which are connected to SELECTOR inputs 13_1-13_4.

Step 8: The PC outputs a value of "1" to 2_2. This disables the DECODER 8 and causes its outputs 9_1-9_8 to assume a value of "1". At the same time the PC also outputs a value of "0" to 2_3. This insures that the CONTROL LATCH 4 clock input 7 is a "0".

Step 9: The PC outputs a value of "1" to 2_3 and a value of "0" to 2_4. This clocks and enables the CONTROL LATCH 4 and causes the value that was output in Step 7 above to be transferred to the corresponding outputs of CONTROL LATCH 4.

Step 10: The PC outputs a value of "0" to 2_2 which enables the DECODER 8. The value of "011" that was transferred to DECODER inputs 11_3-11_1 in Step 9 above causes the DECODER output 9_4 and thus SELECTOR input 14_1 to assume a value of "0". This causes the D0-D3 values on SELECTOR inputs 13_1-13_4 to be gated to SELECTOR outputs 15_1-15_4 and thus PC CONTROL IN terminals 3_1-3_4.

Step 11: The PC reads the data D0-D3 values on PC CONTROL IN terminals 3_1-3_4.

Step 12: The PC outputs a "1" on terminals 1_4 and 1_7. The "1" on 1_7 will be used to raise the /RD line to a "1". The "1" on 1_4 will be used to disable the HIGH ADDR LATCH 17 and the LOW ADDR LATCH 18.

Step 13: The PC outputs a value of "1" to 2_2. This disables the DECODER 8 and causes its outputs 9_1-9_8 to assume a value of "1". At the same time

the PC also outputs a value of "0" to 2_3. This insures that the CONTROL LATCH 4 clock input 7 is a "0".

Step 14: The PC outputs a value of "1" to 2_3 and a value of "0" to 2_4. This clocks and enables the CONTROL LATCH 4 and causes the "1" that was output to 1_4 and 1_7 in Step 12 above to be transferred to outputs 5_4 and 5_7 of CONTROL LATCH 4. The "1" on 5_4 is connected to enable inputs 22 and 25 and thus disables HIGH ADDR LATCH 17 and LOW ADDR LATCH 18. Since 5_7 is connected to the /RD terminal the /RD terminal goes to "1".

What is claimed is:

PRINTER PORT INTERFACE

Abstract of the Disclosure

A printer port interface is provided which converts the printer port on a personal computer to a general purpose bus so that a number of external devices or microprocessor peripheral integrated circuits may be connected to a personal computer via the printer port on the personal computer. This interface enables the printer port to emulate a simple 8 bit microprocessor. The interface device connects the external device to the personal computer and in *write* mode, receives data from the personal computer, signals the external device to accept the information, and sends the data to the external device and in *read* mode signals the external device to provide data, receives data from the external device and sends the data in amounts which do not exceed the input limits of the printer port to the personal computer.

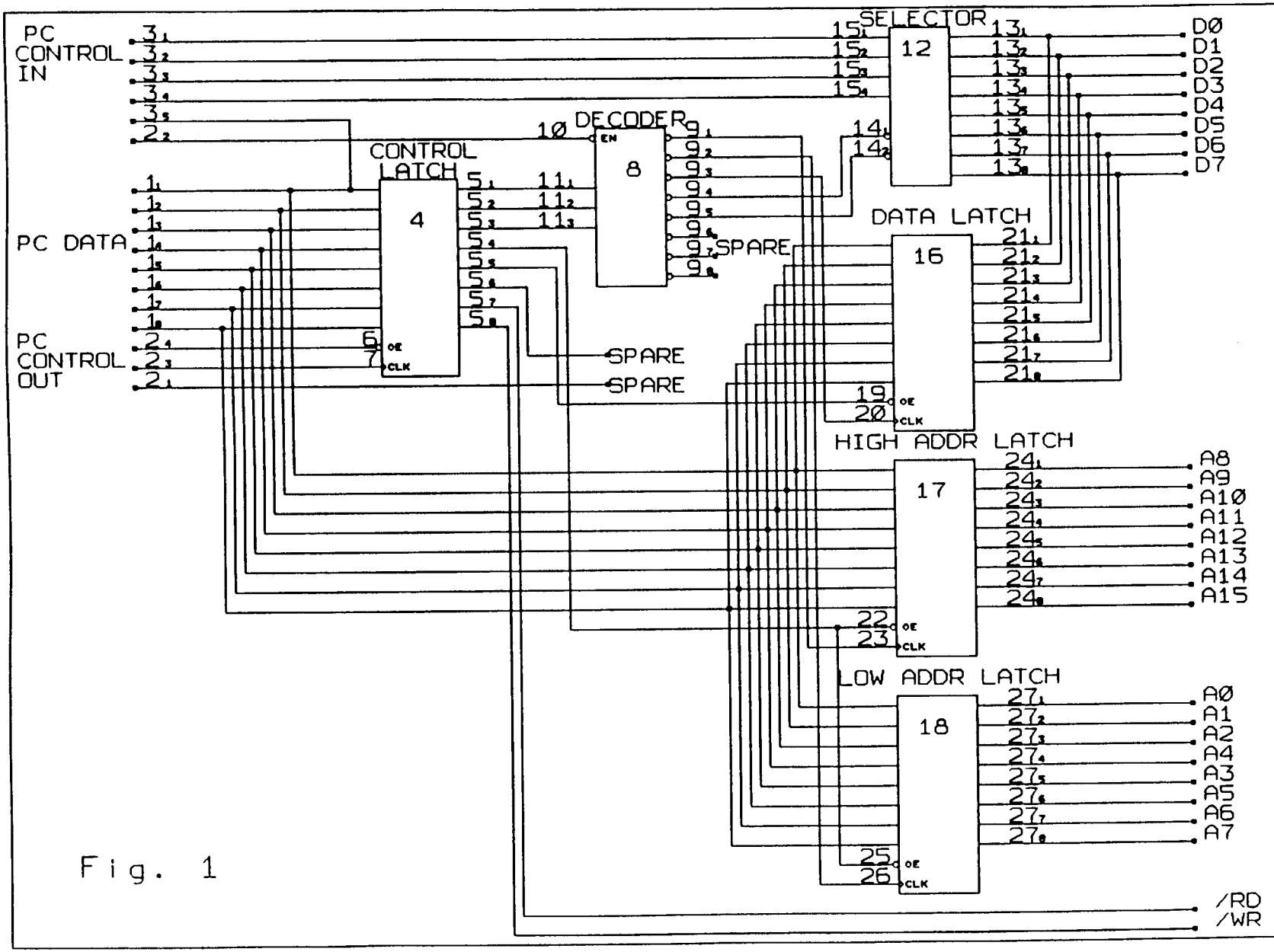

Fig. 1

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