March 2004 • NREL/SR-520-35684

Subcontractor Report

Process R&D for CIS-Based Thin-Film PV

Annual Technical Report
24 April 2002–23 April 2003

D.E. Tarrant and R.R. Gay
Shell Solar Industries
Camarillo, California

National Renewable Energy Laboratory

1617 Cole Boulevard
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Prepared under Subcontract No. ZDJ-2-30630-16

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Preface

Shell Solar Industries (SSI), formerly Siemens Solar Industries has pursued the research and development of $CuInSe_2$-based thin film PV technology since 1980. At the start of subcontract activities with NREL, SSI had demonstrated a 14.1% efficient 3.4 cm^2 active-area cell, unencapsulated integrated modules with aperture efficiencies of 11.2% on 940 cm^2 and 9.1% on 3900 cm^2, and an encapsulated module with 8.7% efficiency on 3883 cm^2 (verified by NREL).

SSI began a 3-year, 3 phase cost-shared subcontract (No. ZN-1-19019-5) on May 1, 1991 with the overall project goal of fabricating a large area, stable, 12.5% aperture efficient encapsulated CIS module by scaleable, low-cost techniques on inexpensive substrates. Subcontract accomplishments were facilitated by addressing module reproducibility using small area test devices and mini-modules. Statistical process control disciplines were adopted to rigorously quantify process reproducibility. SSI addressed uniformity and reproducibility of absorber formation, interactions of the substrate with the absorber, and performance losses near interconnects. Subcontract accomplishments included demonstration of encapsulated module efficiencies that were at that time the highest reported mini-module efficiencies for any thin film technology (encapsulated 12.8% efficient mini-module on 68.9 cm^2 and an NREL-verified 12.7% efficient unencapsulated circuit on 69 cm^2 with a prismatic cover), demonstration of a champion large area (3860 cm^2) encapsulated module efficiency of 10.3% (verified by NREL) that was the first thin film module of its size to exceed the 10% efficiency level, and delivery to NREL of a one kilowatt array of large area (~3890 cm^2) approximately 30 watt modules [1].

From September 1995 through December 1998, SSI participated in a 3-year, 3 phase cost-shared TFPPP subcontract (No. ZAF-5-14142-03). The primary objective of this subcontract was to establish reliable high-throughput, high-yield thin film deposition processes in order to make CIS a viable option for the next generation of photovoltaics. Outdoor testing, accelerated environmental testing, and packaging development progressed throughout all phases of this subcontract. During Phase 1, SSI rigorously demonstrating process reproducibility and yield for a 10x10-cm monolithically interconnected "mini-module" baseline process and demonstrated a 13.6% aperture area efficient mini-module (verified by NREL). During Phase 2, SSI demonstrated the need to replace an existing large area reactor with a reactor based on a more direct scale-up of the baseline reactor, built a new large area reactor, and demonstrated comparable performance for the mini-modules baseline and 28x30-cm circuit plates. SSI developed products and prototype large area modules using a new package designed to integrate small circuit plates into larger modules. A one kilowatt array of $Cu(In,Ga)(S,Se)_2$ modules was delivered to NREL replacing a previously installed array based on an older absorber formation technology without sulfur incorporated in the absorber ($Cu(In,Ga)Se_2$). This array demonstrated significant improvements in efficiency and the temperature coefficient for power. SSI introduced two new 5-watt (ST5) and 10-watt (ST10) CIS-based products designed for use in 12 V systems, and NREL confirmed a new world-record efficiency of 11.1% on a SSI large area (3665 cm^2) module. During subcontract Phase 3, substrate size was scaled from ~30x30 cm to ~30x120 cm and good process control was demonstrated with an average efficiency of 10.8%. Commercial product samples were delivered to NREL and a second set of ~30x120 cm modules (32 modules totaling ~1.2 kW) was delivered to the NREL Outdoor Test Facility. The NREL measured average efficiency at standard test conditions of 11.4% was at that time the highest large area efficiency for any thin-film technology and NREL confirmed a world-record 11.8% large area (3651 cm^2) efficiency for the champion module [2].

From August 1998 through November 2001, SSI participated in a 3-year, 3 phase cost-shared TFPPP subcontract (No. ZAF-5-14142-03). The primary objectives of this "Commercialization of CIS-Based Thin-Film PV" subcontract were to scale-up substrate size and to increase production capacity of the baseline CIS module process while introducing CIS-based products. These objectives were pursued to fabricate efficient and stable thin-film modules made by scaleable, manufacturable, low-cost techniques. An additional mid- to longer-term objective was to advance CIS based thin-film technology thereby assuring future product competitiveness by improving module performance, cost per watt produced, and reliability. Throughout this subcontract, SSI capabilities were leveraged as a Technology Partner participating in NREL team oriented TFPPP activities to address near-term to longer-term R&D topics. SSI's approach to this work was to apply design of experiment and statistical process control methodologies. Siemens Solar was the first company in the world to start production of PV modules based on CIS thin-film technology and this major milestone in the development of PV was recognized by R&D Magazine by awarding the prestigious R&D 100 Award to the Siemens Solar family of CIS solar modules. NREL, the California Energy Commission and SSI shared this award. SSI expanded the CIS product line in 1999 to include 20-Watt "ST20" modules and 40-Watt "ST40" modules. Also during the first subcontract phase, a record-breaking efficiency of more than 12% was verified by NREL for an ST-40 module. This result in 1999 far surpassed the DOE year 2000 goal for a commercial CIS module above 10%. During the second subcontract phase, SSI delivered 20 ST-40 large area modules, all with efficiencies over 11%, to meet the subcontract deliverables defined as large area modules with efficiencies of over 10%. The average efficiency based on a Gaussian fit to the main portion of the circuit plate efficiency distribution was increased from 10.8% prior to this subcontract to 11.6% for this subcontract period. These advancements were due to continuous improvement of all process along with particular attention to process research for two critical processes – CIS formation in new large area reactors and the quality of molybdenum deposited in new high capacity sputtering equipment. Process development improved adhesion, decreased breakage, addressed control of raw materials, and decreased failures associated with patterning. Further R&D of all CIS processes for part size and capacity scale-up was pursued during the third subcontract phase. Major accomplishments included addressing process issues for implementation of high quality high throughput Mo deposition and patterning, high throughput precursor deposition, and higher throughput reaction of the precursor. Circuit plate production capacity was increased by more than an order of magnitude from the beginning of this subcontract while circuit and module efficiencies were steadily improved. The second subcontract milestone – to achieve a pilot production rate 500 kW per year by the end of subcontract – was first achieved in March of 2001 [3].

Acknowledgments

Siemens Solar Industries wishes to acknowledge the contributions of the following people and organizations.

The Siemens Solar Industries CIS Team:

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Brookhaven National Laboratory
Colorado State University
Florida Solar Energy Center
Fraunhofer Institute / GSF
Institute of Energy Conversion / University of Delaware
National Renewable Energy Laboratory
Pennsylvania State University
Showa Shell Seikyu, K.K.
Shell Solar GmbH
Washington State University

Summary

Compared to traditional wafer-based crystalline silicon technologies, monolithic integration of thin film solar cells can lead to products of comparable performance but with significant manufacturing advantages: lower consumption of direct and indirect materials, fewer processing steps and easier automation. Monolithic integration is required to achieve these advantages since this eliminates multiple process steps and handling operations during formation of the absorber and during module assembly. The basic module elements for all thin-film technologies (alloys of amorphous silicon, cadmium telluride and CIS) are the same; the module elements are a circuit-glass/cover-glass laminate, a frame, and a junction box. The basic circuit elements are also very similar; they each have a base electrode, an absorber, a junction, a top electrode and three patterning steps for monolithic integration. While the details of these module elements or equivalent module elements differ, the basic cost structures are very similar on an area-related basis. Since the cost per unit area is the same, the cost per watt is inversely proportional to the module efficiency. CIS cells and monolithically integrated modules have demonstrated the highest efficiencies of any candidate thin-film technologies; therefore, CIS is expected to have the lowest manufacturing cost/watt.

The primary objectives of this subcontract are to:

- Address key near-term technical R&D issues for continued CIS product improvement
- Continue process development for increased production capacity
- Develop processes capable of significantly contributing to DOE 2020 PV shipment goals
- Advance mid- and longer-term R&D needed by industry for future product competitiveness including improving module performance, decreasing production process costs per watt produced, and improving reliability
- Perform aggressive module lifetime R&D directed at developing packages that address the DOE goal for modules that should last up to 30 years while retaining 80% of initial power

Outstanding progress has been made in the initial commercialization of high performance thin film CIS technology. During this subcontract period, predictability of SSI's CIS process was demonstrated by continuously executing the process while increasing throughput. Cumulative production for 2002 exceeded 1 MW - about twice the production rate for 2001. Average laminate efficiency for 2002 is 10.8% with a full width of only 12% of the average. Dramatic increases in line yield were achieved from improved production protocols and by addressing disparate special causes for process variation. Line yield increased from about 60% in 2000 to about 85% in 2002. NREL confirmed a champion 12.8 percent aperture area conversion efficiency for a large area (3626 cm^2) CIS production module. Field failure mechanisms for prototype modules were clearly demonstrated. Additional circuit plate or packaging process variables, although not as clearly established, were also found to effect long-term stability for pre-production modules. Significant progress was made toward developing a "glass/glass" package that eliminates the TPAT backsheet for decreased cost, simplification of the package

and decreased operating temperature. Very promising preliminary results were demonstrated for edge seals developed in collaboration with the new NREL sponsored National Thin-Film PV Module Reliability Team. Long-term outdoor stability has been demonstrated at NREL where ~30x30 cm and ~30x120 cm modules with multiple prototype package designs have undergone testing for over fourteen years.

The demonstrated high line yield is the major accomplishment. No one major process improvement was responsible for the yield improvements. Judicious application of manufacturing engineering disciplines such as SPC, analysis of variation and design of experiments led to a clear definition of near term yield issues. Dramatic improvements in yield were the result of improving production protocols and addressing disparate special causes for process variation. This major accomplishment supports attractive cost projections for CIS. Process R&D at successive levels of CIS production has led to the continued demonstration of the prerequisites for commitment to large-scale commercialization. SSI's thin-film CIS technology is poised to make very significant contributions to DOE/NREL/NCPV long-term goals - higher volume, lower cost commercial products.

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Introduction

Overview

Multinary $Cu(In,Ga)(Se,S)_2$ absorbers (CIS-based absorbers) are promising candidates for reducing the cost of photovoltaics well below the cost of crystalline silicon. CIS champion solar cells have exceeded 18% efficiency for devices fabricated at NREL [4]. Small area, fully integrated modules exceeding 13% in efficiency have been demonstrated by several groups [5]. Record breaking efficiencies of over 12% for a commercial large area module have been verified by NREL [6]. Long-term outdoor stability has been demonstrated at NREL by ~30x30 cm and ~30x120 cm SSI modules which have been in field-testing for over fourteen years. Projections based on current processing indicate production costs well below the cost of crystalline silicon [5].

Compared to traditional wafer-based crystalline silicon technologies, new thin film technologies yield products of comparable performance but with significant advantages in manufacturing [5, 7]:

- Lower consumption of direct and indirect materials
- Fewer processing steps
- Easier automation

Lower consumption of direct and indirect materials results in part from the thin-film structure for the semiconductor used to collect solar energy. All three of these manufacturing advantages are in part due to an integrated, monolithic circuit design illustrated in Figure 1. Monolithic integration eliminates multiple process steps that are otherwise required to handle individual wafers and assemble individual solar cells into the final product.

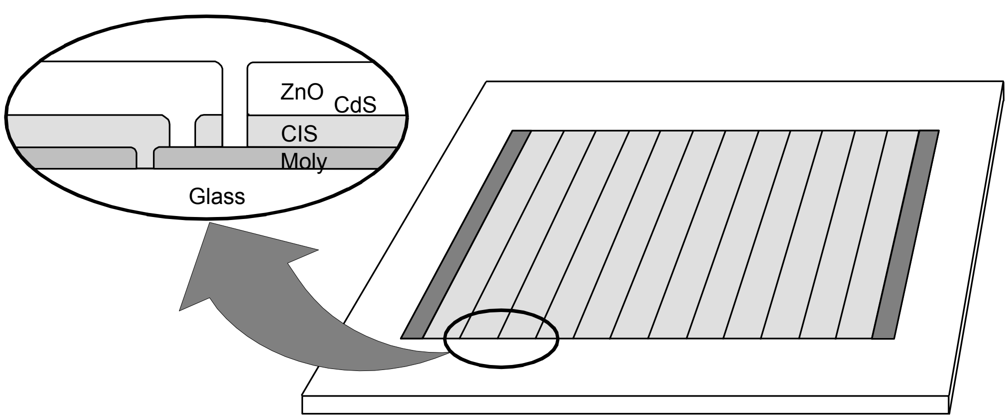


Figure 1. Structure of SSI's monolithically integrated thin-film circuits.

A number of thin film photovoltaic technologies have been developed as alternatives to the traditional solar cells based on crystalline silicon wafers [5]. The technologies with the greatest potential to significantly reduce manufacturing costs are based on alloys of amorphous silicon (a-Si), cadmium telluride (CdTe), CIS, and film silicon (Si-film). These photovoltaic thin film technologies have similar manufacturing costs per unit area since all share common elements of design and construction:

- Deposition of typically three layers on a suitable substrate – window/electrode, absorber, and back electrode
- Patterning to create monolithically integrated circuit plates
- Encapsulation to construct modules

Cost per watt is a more appropriate figure of merit than cost per unit area [5]. All thin film technologies have similar manufacturing costs per unit area since they all use similar or equivalent deposition, patterning, and encapsulation processes. About half of the total module cost – material, labor, and overhead – originates in the encapsulation scheme which is for the most part independent of the thin film technology. Costs for alternative encapsulation schemes are typically similar or even higher. The average efficiency of large, ~30x120 cm modules in pilot production at Siemens Solar is approximately 11%. This performance is comparable to many modules based on crystalline silicon, and is substantially better than the performance reported for competing thin-film technologies. The lowest cost per peak watt will result from the technology with the highest efficiency, CIS technology, since most thin film technologies have similar cost per unit area.

SSI CIS Process

Most terrestrial photovoltaic products today are designed to charge a 12-volt battery, however the output voltage of an individual solar cell is typically about 0.5 volts. Wafer-based technologies build up the voltage by connecting individual solar cells in series. In contrast, CIS circuits are fabricated monolithically (Figure 1); the interconnection is accomplished as part of the processing sequence to form the solar cell by alternately depositing a layer in the cell structure and patterning the layer using laser or mechanical scribing.

The structure of a SSI CIS solar cell is shown in Figure 2. The full process to form CIS circuit plates, including monolithic integration, is outlined in Figure 3. This process starts with ordinary sodalime window glass, which is cleaned and an SiO_2 barrier layer is deposited to control sodium diffusion and improve adhesion between the CIS and the molybdenum (Mo) base electrode. The Mo base electrode is sputtered onto the substrate. This is followed by the first patterning step (referred to as “P1”) required to create monolithically integrated circuit plates – laser scribing to cut an isolation scribe in the Mo electrode. Copper, gallium and indium precursors to CIS formation are then deposited by sputtering. Deposition of the precursors occurs sequentially from two targets in an in-line sputtering system, first from a copper-gallium alloy target (17 at% Ga) and then from a pure indium target. CIS formation is accomplished by heating the precursors in H_2Se and H_2S to form the CIS absorber. Beginning at room temperature, furnace temperature is ramped to around 400ºC for selenization via H_2Se, and ramped again to around 500ºC for subsequent sulfidation via H_2S, followed by cool-down to room temperature. This deposition of copper and indium precursors followed by reaction to form CIS is often referred to as the two-stage process. A very thin coating of cadmium sulfide (CdS) is deposited by chemical bath deposition (CBD). This layer is often referred to as a "buffer" layer. A second patterning step (P2) is performed by mechanical scribing through the CIS absorber to the Mo substrate thereby forming an interconnect via. A transparent contact is made by chemical vapor deposition (CVD) of zinc oxide (ZnO). This layer is often referred to as a "window layer" or a transparent conducting oxide (TCO). Simultaneously, ZnO is deposited on the exposed part of the Mo substrate in the interconnect via and thereby connects the Mo and ZnO electrodes of adjacent cells. A third and final patterning step (P3) is performed by mechanical scribing through the ZnO and CIS absorber to isolate adjacent cells.

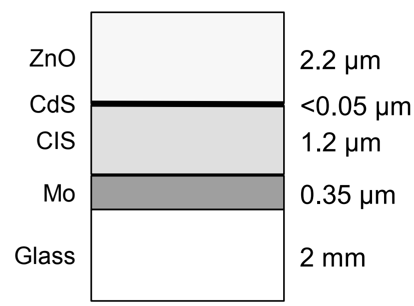


Figure 2. SSI's CIS cell structure (not to scale).

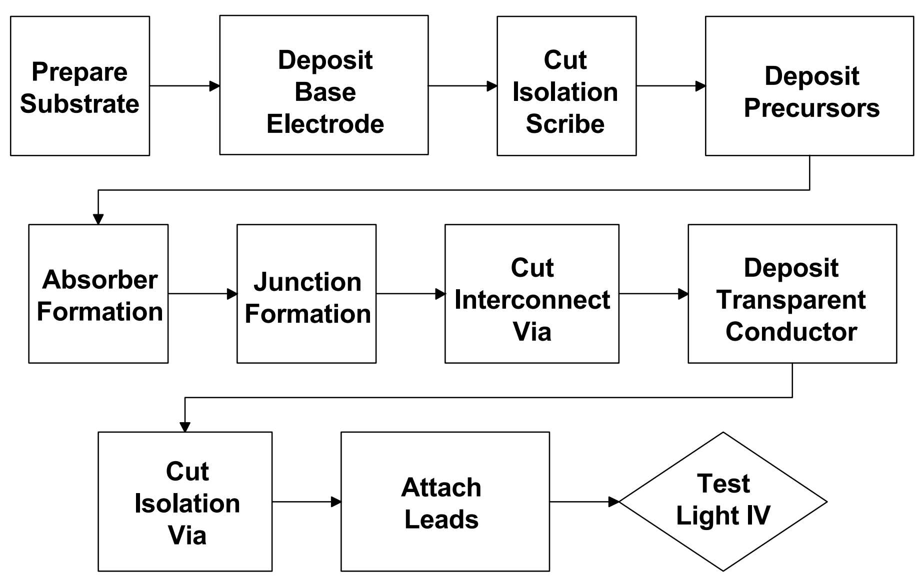


Figure 3. SSI CIS Circuit Processing Sequence.

The CIS-based absorber referred to in this report is composed of the ternary compound $CuInSe_2$ combined with sulfur and gallium to form the multinary compound $Cu(In,Ga)(S,Se)_2$. Gallium and sulfur are not uniformly distributed throughout the absorber but the concentrations are graded; hence, this structure is referred to as a "graded absorber." The graded absorber structure is a graded $Cu(In,Ga)(Se,S)_2$ multinary with higher sulfur concentration at the front and back and higher Ga concentration at the back. Elemental profiles typical of the SSI graded absorber structures are presented in Figure 4. Efficiency, voltage, and adhesion improvements have been reported for the SSI graded absorber structure [1, 8, 9].

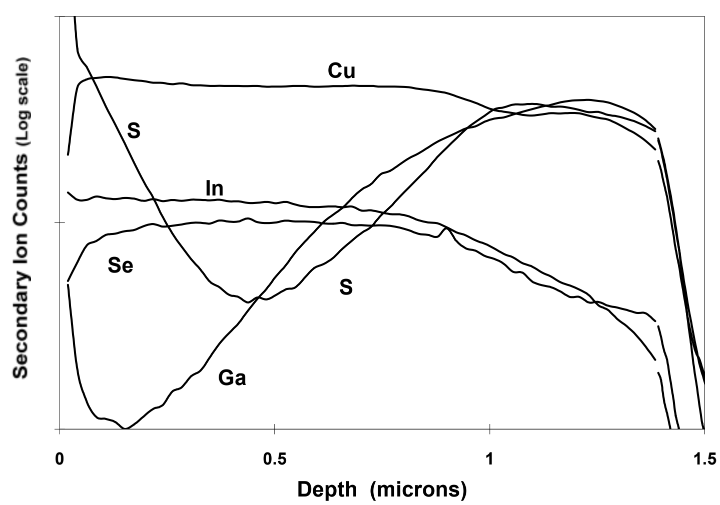


Figure 4. Typical elemental profile for the SSI graded absorber (SIMS from NREL).

Figure 5 illustrates the module configuration used for prototypes and ST products during this subcontract period. EVA is used to laminate circuit plates to a tempered cover glass and a Tedlar/polyester/Al/Tedlar (TPAT) backsheet provides a hermetic seal. Aluminum extrusions are used to build frames for the modules. In addition to providing a hermetic seal, the combination of the TPAT backsheet and the offset between the circuit plate and the frame provides electrical isolation from the frame.

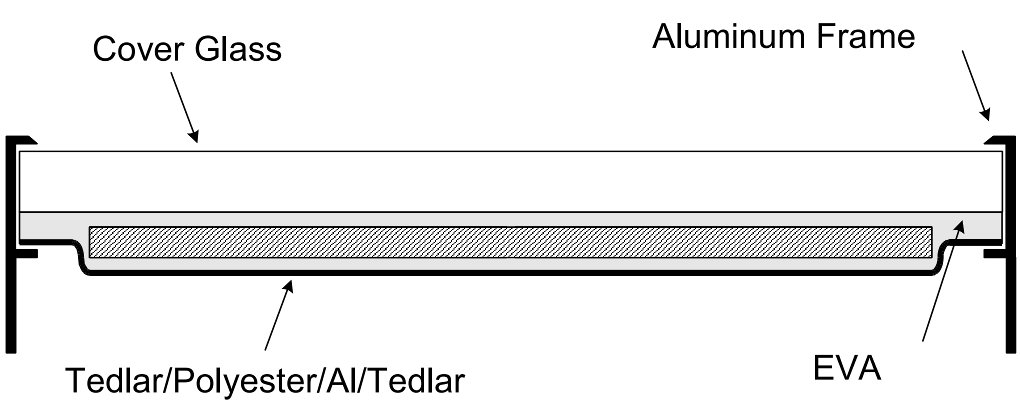


Figure 5. Single circuit plate module configuration with a TPAT backsheet.

SSI's R&D Approach

From the industrial perspective, the full process sequence anticipated for use in large-scale production must be mastered and rigorously demonstrated. The SSI research approach is composed of two main elements:

- Experimentation and development using device structures that exercise all aspects of large area module production [10]
- Application of statistical process control (SPC) as the discipline to rigorously quantify process reproducibility, and application of statistical methods such as analysis of variation (ANOVA) to rigorously quantify experimental results [11, 12].

Process predictability is a prerequisite for commercialization of thin-film PV since product performance ratings, yields and costs must be known before committing to produce products. Also, process predictability is essential for proper interpretation of process development efforts since experimental results may be ambiguous or misleading if compared to an unpredictable baseline process. SSI has adopted SPC methodologies because SPC was developed to rigorously quantify process reproducibility and process capability; the essence of SPC is predictability. Equally significantly, SPC provides the measure of systematic progress as processes are developed. Communication of this progress is typically best expressed in the language of the SPC discipline [13]. For example, process characterization results are demonstrated to be "statistically significant" based on knowledge of process repeatability measured using the SPC discipline and compared to a predictable baseline process. Confidence in the appropriate interpretation of experimental results is gained through application of statistical methods such as ANOVA to demonstrate statistically significant results.

Subcontract Activities and Milestones

Background

The purpose of the Thin-Film Photovoltaics Partnerships Program (TFPPP) is to accelerate the progress of thin film solar cells and module development as well as to address mid and long-term research and development issues. The long-term objective of the TFPPP is to demonstrate commercial, low-cost, reproducible, high yield and robust modules of 15% aperture-area efficiency. Further more, this research is directed at making progress toward this objective by achieving interim goals in thin film module efficiencies; cell and module processing; cell and module reliability and the necessary fundamental research needed to build the technology base that support these key areas. Participation in the National R&D Teams is paramount to the success of this project. The DOE/NREL/NCPV strategy in undertaking this R&D effort is to maintain the good coupling between laboratory results from fundamental materials and processes research to manufacturing R&D, pilot-line operation, and early entry of advanced thin-film PV products to the ever-growing marketplace worldwide.

The purpose of this subcontract, as part of the Technology Partners Category, is to accelerate the progress of thin film solar cell and module development as well as to address mid and long-term research and development issues by achieving aggressive interim goals in thin film module efficiencies; cell and module processing; cell and module reliability; and in the technology base that supports these key areas.

Objectives

The primary objectives of this subcontract are to:

- Address key near-term technical R&D issues for continued CIS product improvement
- Continue process development for increased production capacity
- Develop processes capable of significantly contributing to DOE 2020 PV shipment goals
- Advance mid- and longer-term R&D needed by industry for future product competitiveness including improving module performance, decreasing production process costs per watt produced, and improving reliability
- Perform aggressive module lifetime R&D directed at developing packages that address the DOE goal for modules that should last up to 30 years while retaining 80% of initial power

Milestones

SSI shall perform each of the above tasks with the goal of meeting the following targets:

- Scale the substrate size from 1 ft. X 4 ft. to approximately 2 ft. X 5 ft. by the end of the subcontract.
- Achieve pilot production rates of 9,000 kW per year by the end of the subcontract.
- Demonstrate commercial, low-cost, reproducible, high yield and robust module process that achieve the DOE goal for 15% aperture-area efficiency
- Deliverables for the subcontract include CIS-based products and representative modules delivered to the NREL Module Testing Team for outdoor testing and evaluation.

Deliverables

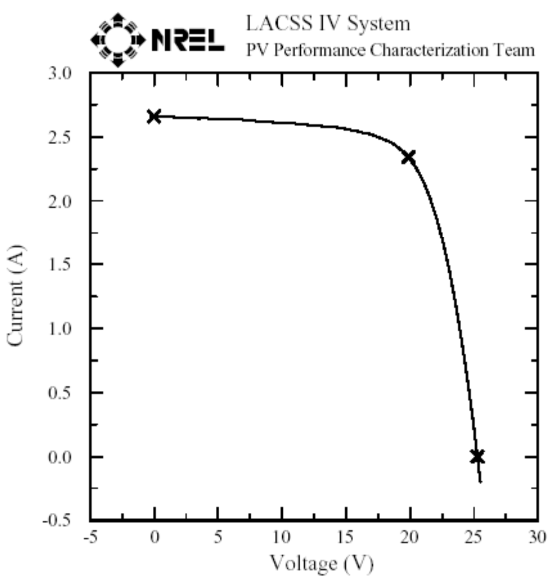
SSI will deliver 10 representative CIS-based module products at the end of each phase of the subcontract.

SSI will deliver 10 representative CIS modules to the NREL Module Testing Team by the end of each phase of the subcontract.

Technical Review

Process R&D

NREL has confirmed a champion 12.8 percent aperture area conversion efficiency for a large area (3626 cm^2) CIS module (Figure 6). The aperture area for this champion module was defined by taping off the approximately 1 cm inactive boarder surrounding the monolithically integrated CIS circuit in a ST40, 40 W, production module. Other than definition of the aperture area, this module is simply one module from the upper end of the production distribution for standard modules.



	Module	per Cell	
Eff	12.8		%
Voc	25.3	0.601	V
Isc	2.7		A
Jsc		30.8	mA/cm^2
FF	69.2		%
Area*	3626	86.3	cm^2
Cells	42		

* Aperture area - including interconnect loss

Figure 6. Champion ST40 module from the upper end of the production distribution.

Figure 7 is the production distribution for approximately sixteen thousand ~1x4-ft. laminates produced during 2002. The average efficiency of this distribution is 10.8%. A Normal distribution fit to the main portion of the distribution yields a standard deviation of 0.66%; over 88% of this production output is over 10% efficiency.

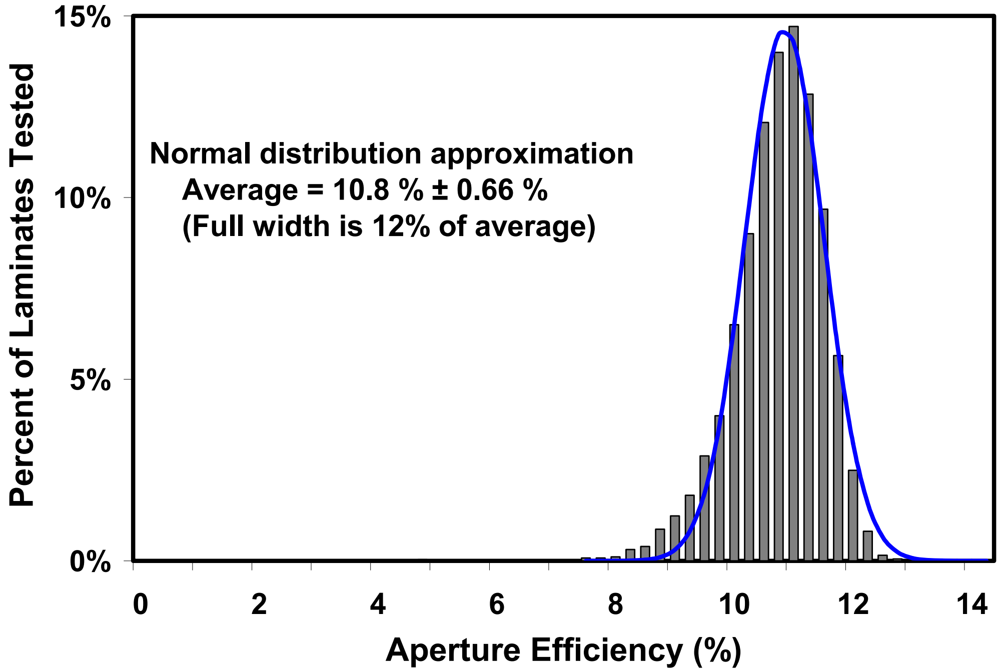


Figure 7. Production distribution for 1x4-ft. laminates produced during 2002

These champion efficiency and production distribution results are particularly notable since they were achieved along with a cumulative production for 2002 of over 1 MW; almost twice the production rate for 2001. Historical production rates and the production rate achieved during 2002, nominally the first phase of this subcontract, are charted in Figure 8.

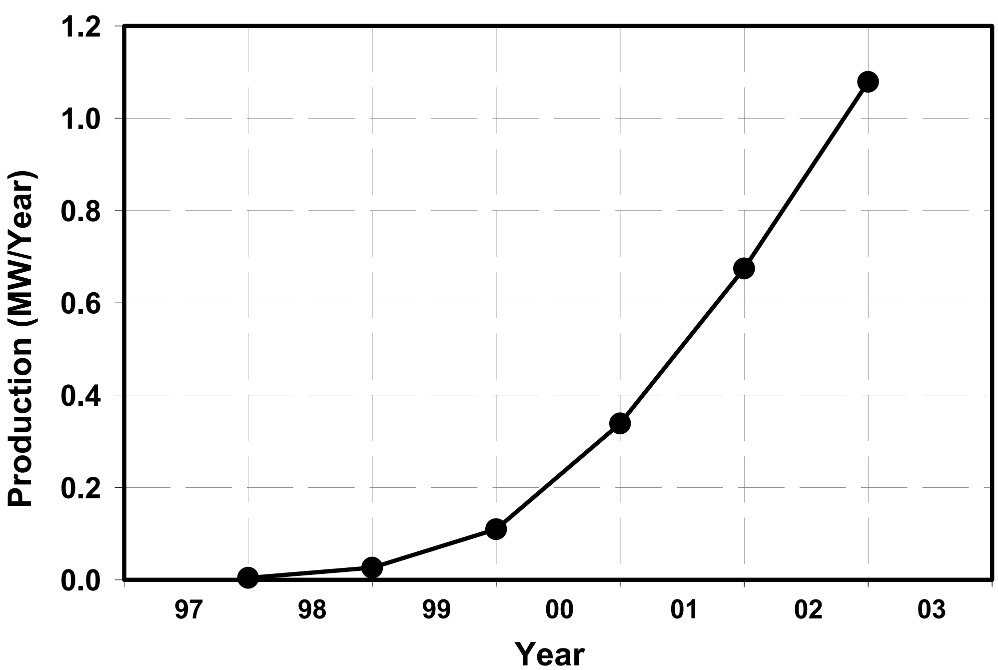


Figure 8. Historical production rate including the first phase of this subcontract (2002).

Dramatic increases in CIS line yield have been demonstrated [14, 15]. Line yield is defined as the ratio of two areas – the area of product produced divided by the area of glass started through the production line. This is total yield including both electrical yield and mechanical yield through all processing required to produce products. Line yield has increased from about 60% in 2000 to about 85% in 2002. Process development, guided by SPC approaches, for all process steps was required to achieve this high yield. This major accomplishment supports attractive cost projections for CIS.

Figure 9 illustrates yield improvements over approximately the last three years. No one major process improvement was responsible for demonstrated yield improvements. Instead, these advancements were due to continuous improvement of multiple processes.

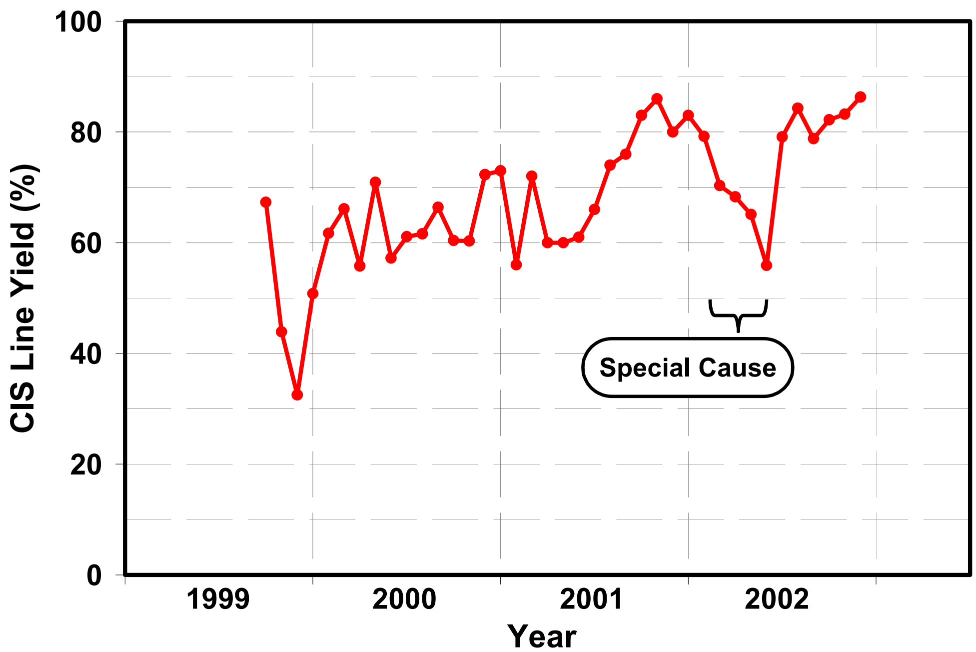


Figure 9. Yield improvements.

Judicious application of manufacturing engineering disciplines such as SPC, analysis of variation and design of experiments led to a clear definition of near term yield issues. Based on this guidance, the dramatic improvements in monthly yield through this timeframe were the result of improving production protocols and addressing disparate special causes for process variation. Significant improvements were made by developing protocols and procedures for sun soaking modules prior to final testing. Yield improvements as the result of process development included:

- Decreased breakage at multiple process steps related to handling and process definition

- Elimination of shunting along the laser scribe in the Mo base electrode related to both the Mo deposition and laser patterning processes
- Decreased loss due to equipment failures by improving control systems and production procedures
- Decreased peeling related to glass cleaning, precursor deposition, the reaction process, reactor uniformity, and ZnO deposition
- Decreased peeling related to glass cleaning
- Decreased peeling related to precursor deposition
- Decreased peeling related to reaction process conditions
- Decreased peeling related to reactor uniformity
- Decreased peeling related to ZnO deposition
- Decreased loss of process runs by improving infrastructure for higher capacity and yield

These yield improvements were obtained through repeated cycles of learning. For example, improper execution for multiple process steps can lead to peeling. The drop in yield through the first half of 2002, Figure 9, was due to peeling. This was found to be due to setup and wear issues for a glass washer; issues that are obvious and trivial in hindsight. Finding and addressing this special cause lead to the immediate and permanent return to high yield.

As an example of subcontract work leading to yield improvements, process development led to yield improvements for newly implemented equipment [16]. SSI defined the requirements and procured laser barcode scribing and barcode reading equipment with the goals of increasing capacity by improving productivity and providing high quality data for integrated manufacturing infrastructure. Figure 10 illustrates the corner of a circuit plate with both a readable serial number for humans and a 2-dimensional barcode for machines.

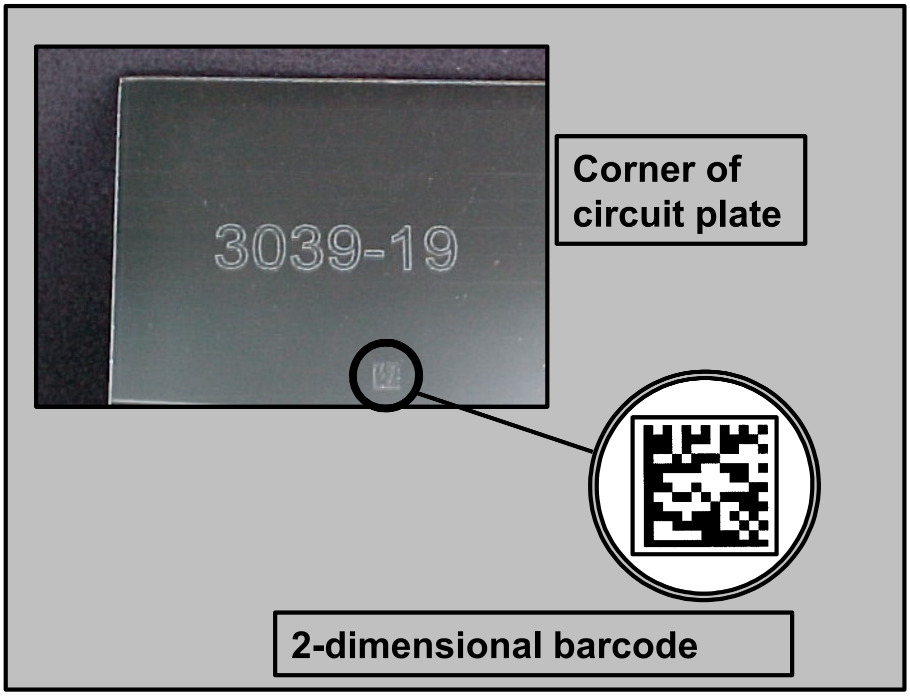


Figure 10. Laser scribed readable serial number and a 2-dimensional barcode.

Process development demonstrated reduced breakage when laser bar codes scribing replaced hand scribed serial numbers. A study of yield loss due to breakage during the absorber formation process demonstrated that breakage associated with hand scribed serial numbers was one of the major causes of breakage. The use of laser scribed bar codes has reduced this kind of breakage by 88%.

National CIS R&D Team

Prior to and during this subcontract phase SSI contributed to TFPPP National CIS R&D Team. Summarizing results for all of the extensive team member activities is not attempted in this report since the expertise for most team activities resides with the team members. Instead, the following joint NREL/SSI experiments are summarized as examples of teamwork where SSI has had major involvement in sample preparation or data analysis. Team activities included:

- SSI supplied two types of SSI thin-films to TFPPP absorber team members - complete through $Cu(In,Ga)(Se,S)_2$ absorber formation and complete through ZnO deposition. These films were supplied for electrical characterization at NREL and IEC, and for compositional analysis at NREL, FSEC, and the University of Illinois.

- SSI supplied thin-films complete through $Cu(In,Ga)(Se,S)_2$ absorber formation for buffer layer experiments at NREL and IEC.

- SSI deposited CVD ZnO on multiple sets of samples from Larry Olsen, WSU.

- SSI supplied samples of precursors for reaction pathway measurements at Oak Ridge National Laboratories to Suku Kim who is in Tim Anderson's group at the University of Florida.

- SSI received data from the CIS array at the NREL OTF from Jill Adelstein. A summary of this data was included in the final report for the previous subcontract.

- SSI attended the National CIS R&D Team Meeting held in conjunction with the IEEE PV Specialists Conference.

- Steve Voss represented SSI at the first meeting of the newly formed National Thin Film Module Reliability Team Meeting which started with a workshop on moisture ingress. Steve presented a talk titled "Accelerated Environmental Testing of Shell Solar CIS"

- SSI participated in team experiments related to identifying the reasons for inconsistent performance for SSI absorber only when devices are made with buffer and ZnO depositions by NREL or IEC. SSI supplied additional samples of thin-films complete through Cu(In,Ga)(Se,S)2 absorber formation for buffer layer experiments at NREL and IEC.

- SSI prepared to supply samples for work on barrier coatings by Larry Olsen at PNNL.

Package Development

Glass/Glass Package

SSI is now developing a "glass/glass" package that eliminates the TPAT backsheet for decreased cost, simplification of the package and decreased operating temperature. Figure 11 is a sketch of the present production package and the proposed glass/glass package. Simplification of the package should increase yield. Decreasing the operating temperature will lead to higher efficiency for modules in the field.

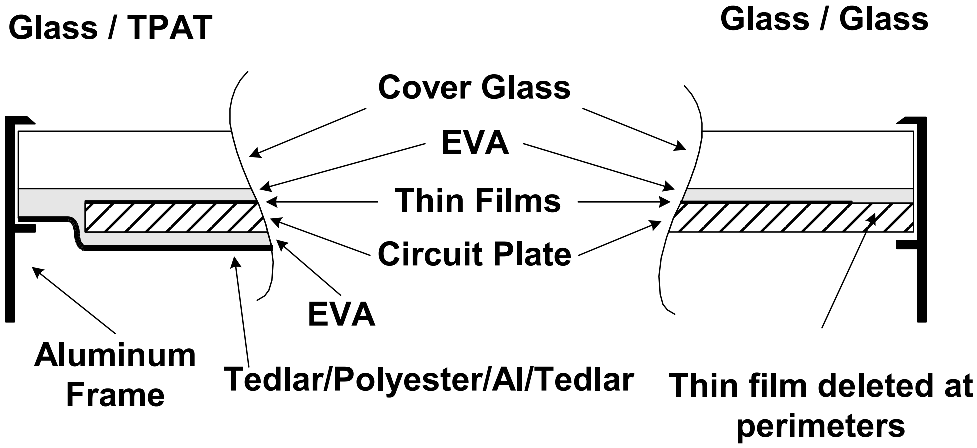


Figure 11. Present and future package designs.

No detectable humidity ingress occurs during damp heat testing of the current SSI products with a TPAT backsheet where damp heat testing refers to an exposure for 1,000 hour at 85ºC and 85% relative humidity. The new glass/glass package is required to pass accelerated environmental tests such as this damp heat test; however, package development indicates that this will require additional moisture protection. Figure 12 is a photo of the edge of a glass/glass module where the interconnect patterning for monolithic integration is visible as vertical lines above the ruler. Darkening and broadening of the interconnects at the edge of the circuit plate is observed for glass/glass packages after damp heat testing and has been found to be an indicator of power loss due to moisture ingress [17]. This is not observed for the glass/glass package after the same thermal exposure but without high humidity. Similarly, the darkening and broadening of the interconnects is not observed for production products, that employ a TPAT backsheet and frame, after the same thermal exposure with or without high humidity. Edge seal and barrier coatings to block humidity ingress are being explored at SSI and in collaboration with the new NREL sponsored National Thin-Film PV Module Reliability Team. Preliminary results are very promising.

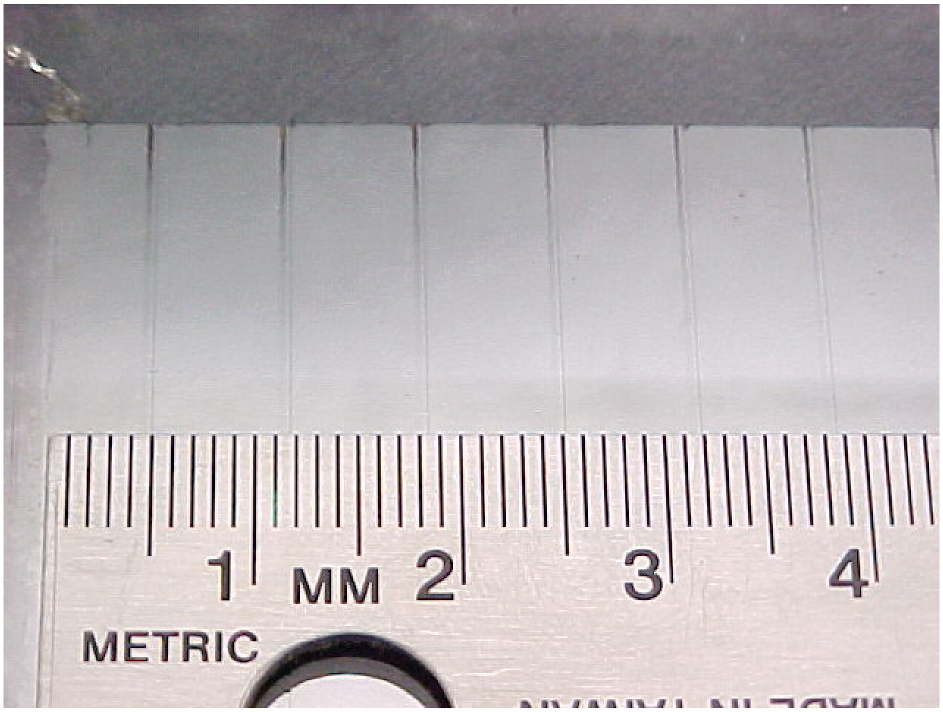


Figure 12. Darkening and broadening of the interconnects due to moisture ingress.

Outdoor testing

FM and UL approval has been obtained for the present package used for the ST series of products and the performance of the ST family of CIS thin-film products is backed by a 10-year warrantee. Present and potential packages are subjected to both accelerated testing and long-term outdoor testing to develop and improve low cost yet durable packages. One way NREL supports SSI in developing products for long-term outdoor reliability is through long term testing of arrays and individual modules at the NREL Outdoor Test Facility (OTF). As depicted in Figure 13, long-term outdoor stability has been demonstrated at NREL where ~30x30 cm and ~30x120 cm modules with multiple prototype package designs have undergone testing for over fourteen years.

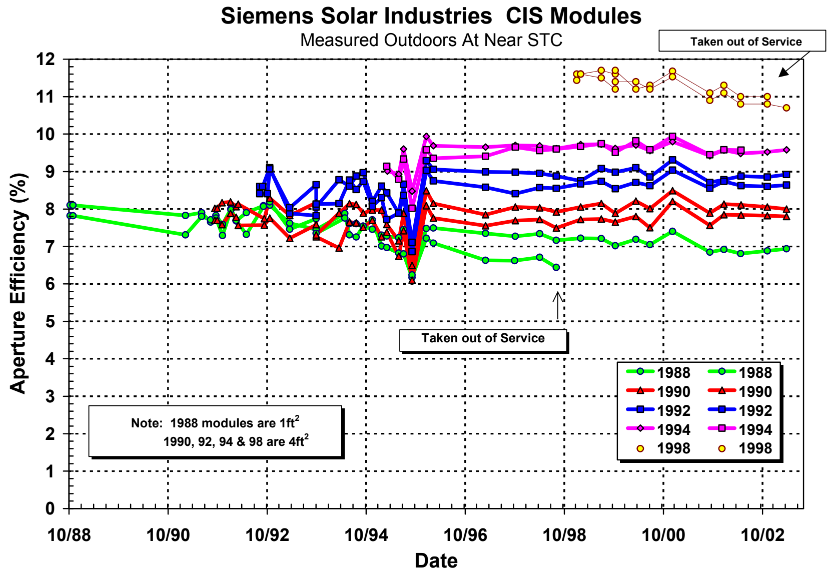


Figure 13. Demonstrated long-term outdoor stability.

SSI has supplied modules to the NREL OTF for three 1kW arrays. In each case, a newer generation of modules has been used to replace older designs using the same test site. The first two arrays demonstrated stability and that thermally induced transients, which are observed after exposure to high temperatures during accelerated environmental testing, are not observed in the field despite daily and seasonal changes in module temperature. This is entirely reasonable since known transient effects are temperature dependent and the module temperatures reached for actual deployment are less than the temperatures defined for accelerated testing.

Data acquisition began on November 18, 1998 for the third 1kW array of modules. The system is comprised of 28 modules with an average efficiency of 11.4% at STC. The aperture area of each module is $0.3651m^2$ and of the total array is $10.2\ m^2$. The array is fixed at a 40° tilt aligned true south and is connected to a resistive load through three maximum power trackers. Continually logged data is corrected for temperature. Only data for incident solar irradiance of between 950-1050 W/m^2 is used for array characterization. NREL measurements indicated array performance, normalized to standard test conditions, over 1kW.

NREL data from late February of 2000 indicated stability within 2% of the measurements made shortly after array deployment. Similarly, data for operation through June 30, 1999 indicated that the array remained stable with array performance over 1kW. As for previous arrays, both module and the array data show good stability with no seasonal variation in performance. It can not be overemphasized that multiple studies have demonstrated that thermally induced transients, which are observed after exposure to accelerated environmental testing conditions, are not observed in the field.

More recent continuously logged data from the OTF indicates that the latest array is now exhibiting changes with time. To follow-up on this observation, NREL made outdoor measurements (Daystar) on each module in the array. Six modules were selected for further study as representative of the varying of degrees power loss for all array modules. NREL provided pulsed simulator (SPIRE), continuous illumination simulator (LACSS), and outdoor measurement (SOMS) data for the six selected modules (). This data indicates that changes in performance are primarily changes in FF. This data also indicates, as is typical of CIS transient effects, observed changes are smaller for measurements made with continuous illumination than for pulsed simulation. For this sample of six representative modules, the change in FF is highly variable ranging from 4% to 18%. The low end of this range is virtually no loss, i.e. within measurement variability. The high end of this range is significant and indicated the need for additional follow-up.

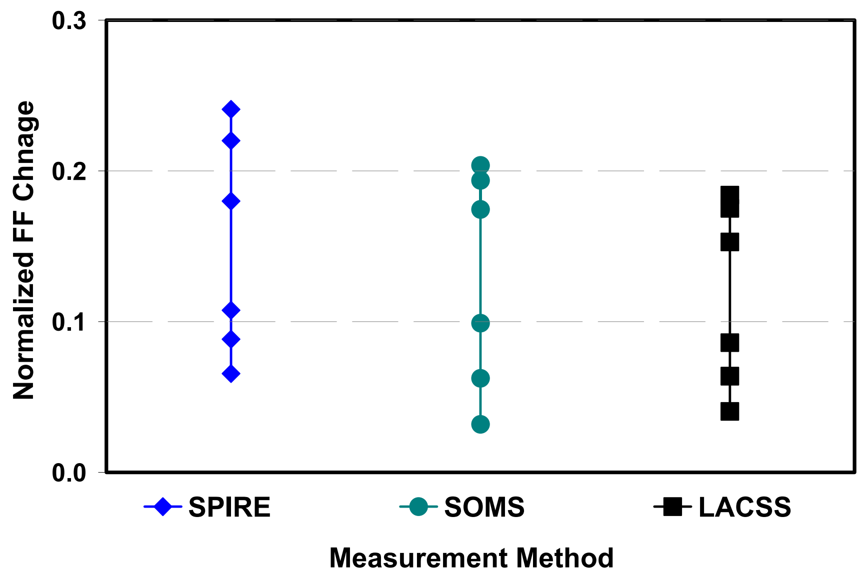


Figure 14. Normalized changes in FF, ranging from virtually no loss to significant losses, for six representative array modules.

Packaging development from early work with mini-modules through ST products has demonstrated that thermally induced losses from lamination or accelerated testing will recover with extended outdoor exposure [3]. SSI has also demonstrated multiple packaging designs, with and without EVA, that protect circuit plates from water vapor ingress during damp heat accelerated testing; exposure for 1000 hour at 85ºC and 85% relative humidity [2, 3]. CIS circuit plates in packages that provide protection from water vapor ingress will pass accelerated environmental tests with an outdoor exposure to reverse thermally induced transient effects. This conclusion was supported by studies by the NREL TFPPP "Transient Effects Group." The team defined a repeatable measurement methodology for systematic study of thermal transient effects that was used to demonstrate reversibility through multiple thermal cycles and thereby support outdoor testing results that indicate long term stability for normal operating conditions [3, 18]. Based on this foundation, SSI testing indicates that no significant humidity ingress occurs during damp heat testing of current SSI products with a TPAT backsheet. Figure 15 is a chart of average efficiency for two groups of 8 modules. One group went through the damp heat environmental test and the other went through the same temperature cycle but without humidity [17]. Both groups were then placed outdoors for 8 weeks of recovery. The two groups show the same thermally induced loss and recovery with light exposure; humidity has no impact on the results for current SSI products.

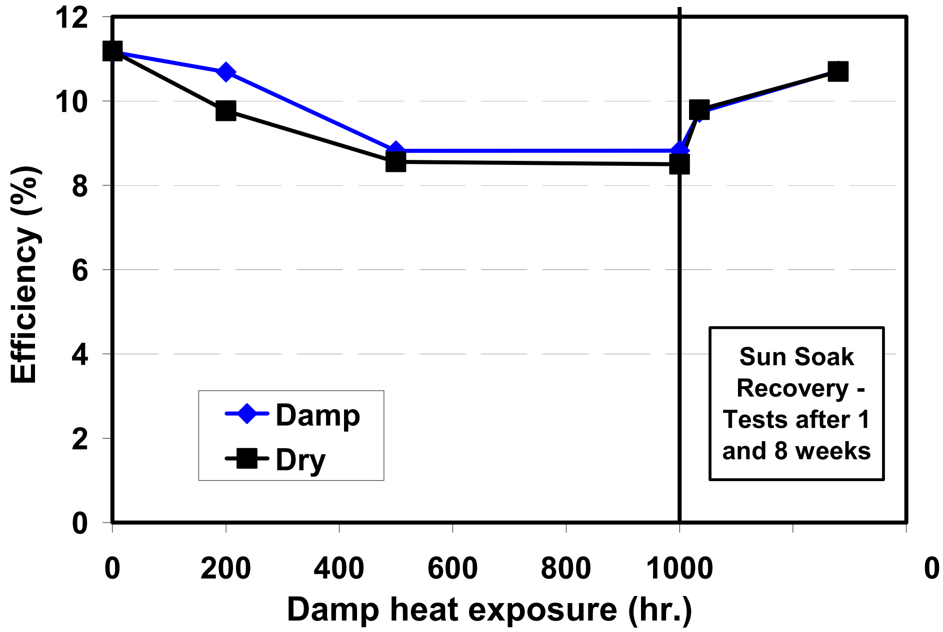


Figure 15. Recovery after the thermal exposure of damp heat accelerated tests with or without including high humidity in the tests.

A significant effort has gone into exploring the apparent inconsistency between the most recent results from the most recent array of prototype modules deployed at NREL, the most recent demonstration of stability for production modules based on accelerated testing, and the combined knowledge from multiple sets of accelerated test results, multiple generations of modules deployed at NREL and the two previous arrays deployed at NREL that were stable. SSI has deployed modules, typically in 1 kW arrays, at test sites throughout the country and, to a lesser degree, throughout the world. Modules from multiple sites were retrieved for nondestructive and destructive testing to explore the observations from the most recent NREL array.

Early prototype module designs included a wide frame that extended across the front of the modules to cover buss bars. CIS modules have an esthetically pleasing uniform nearly black appearance. However, the simplest form of bus bar is a shinny tin-coated copper ribbon. This might be an esthetically pleasing combination if the bus bars were uniform but the shinny solder used to attach the bus bars yields ragged rather than uniform lines. Wide frames were used in pre-production modules to cover the shinny bus bars and solder. The inside edge of these wide frames is very close to the outer cells that are narrow strips extending the length of the module; parallel with and close to the wide frame. This geometry proved to be very sensitive to dirt buildup, Figure 16, in a narrow strip at the edge of frame that shadowed the outer cells. Improved performance was demonstrated after scraping away the dirt. However, not all of the subset of modules that showed degradation fully recovered after scraping away the dirt. Dirt clearly can degrade performance but this mechanism does not explain all degradation. It is assumed that the wide frames also tended to trap water, which also could have lead to degradation.

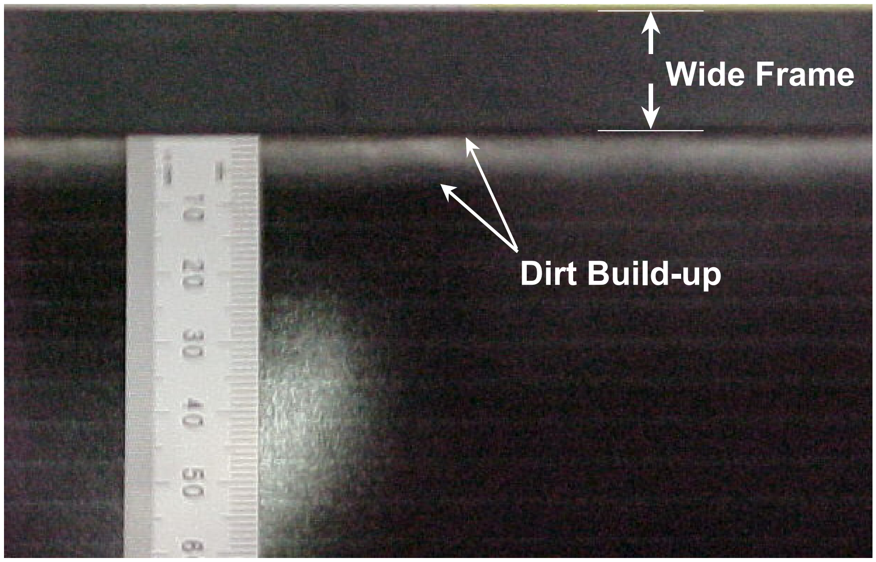


Figure 16. Dirt buildup in a narrow strip at the edge of a wide frame.

Additional testing demonstrated that errors during fabrication caused degradation for some modules and may account for some of the observed OTF array results. In another generation of modules, a uniform dark appearance for the front of modules was achieved with narrow frames by covering the shinny bus bars with black decorative tape prior to encapsulation. For wide or narrow frames, additional tape is used during lay-up for encapsulation to preposition and hold the circuit plate, EVA, glass cover sheet and TPAT backsheet. The proper approach is to tape together the external components, backsheet to the cover glass, thereby holding all components together and allowing the tape to be removed after lamination. However, destructive testing found that this tape was at times improperly used to hold internal components i.e. internal components were taped to the circuit plate or cover glass before laying up the complete package. Therefore, this improperly used tape was partly inside the package during lamination and the tape could not be removed after lamination. Instead, after lamination the tape was trimmed off with the excess EVA and backsheet. The bond between EVA and the adhesive has never been tested for it's ability to prevent water vapor ingress and EVA does not stick at all to the other side of this tape. Therefore, the improperly used tape for lay-up provided a path for water vapor penetration past the hermetic seal formed by the combination of the TPAT backsheet and an offset between the circuit plate and the frame (see Figure 5). The combination of improperly used tape during laminate lay-up and dirt buildup on obsolete wide frames could explain performance variation from virtually no loss to significant losses.

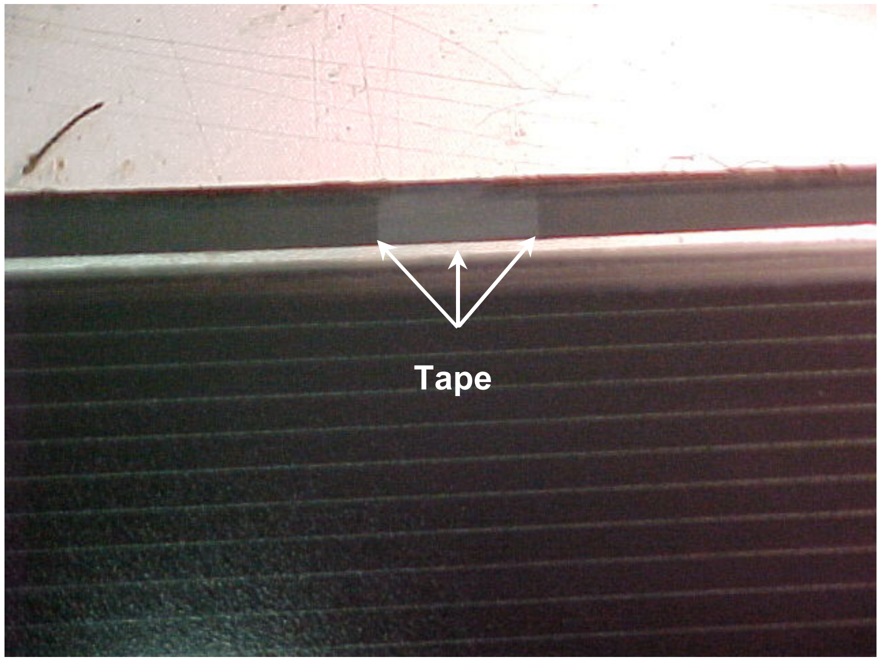


Figure 17. Improperly used tape inside the package.

One of the modules from the array at NREL that showed a degraded FF was dissected expecting that lay-up tape would be found and explain the loss in FF. The frames were removed and the edge of the laminate was inspected. Although indentations in the backsheet due to proper use of lay-up tape were found, inspection of the edge gave no indication of improperly used lay-up tape. The EVA was cut and removed from the step formed by the edge of the circuit plate and the front plate thereby exposing the edge of the laminated circuit plate. No areas of poor adhesion between the EVA and the back edge of the circuit plate were observed by attempting to lift the EVA with a utility knife. This testing indicted no improper use of lay-up tape for this particular module.

Adhesion between the backsheet and the circuit plate was also tested by cutting into the EVA parallel to the circuit plate to release a section of the backsheet and then peeling back the backsheet. Lower adhesion of the TPAT along one of the long edges of the circuit plate was observed along with the odor of EVA. These subjective observations may indicate incomplete curing of the EVA leading to lower interface adhesion and thereby higher moisture ingress. Also, glass to EVA adhesion is know to be dependent on EVA curing and the bond between EVA and glass is mechanical rather than chemical although "primers" are added to the EVA to improve adhesion. In addition to EVA curing, EVA quality, priming, glass surface quality or other lamination and packaging issues could have lead to the lower adhesion of the TPAT along one edge and the odor of EVA. In addition, the ability of the frames to help maintain a physical bond through compression, directly inhibit water vapor penetration or avoid trapping water may depend on these packaging details and the indentations in the backsheet from "proper" use of lay-up tape. Therefore, packaging issues, the use of lay up tape and other details of the lamination and framing processes, may have contributed to failure for some but not all modules.

Laser scanning results published by NREL indicate degradation due to shunting primarily at the edge of modules, which is consistent with an interpretation that packaging issues lead to degradation [19]. Reverse bias hot spot measurements made at NREL using a technique based on observing discoloration of heat sensitive sheets indicated hot spots throughout some degraded modules. However, a correlation between the qualitative hot spot data and the modules that degraded could not be established since similar data before degradation was not available, the link between forward bias FF and reverse bias hot spots is tenuous, and a comparison could not be made between hot spots and modules with and without degradation. These hot spot measurements do not seem to clearly contradict the laser scan results indicating a packaging issue.

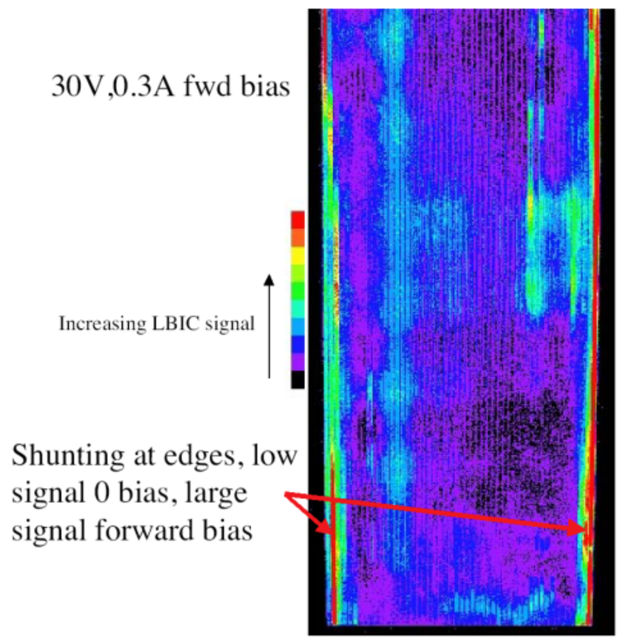


Figure 18. A laser scan of a thin-film module showing shunting at the edges (Figure 8. from reference 19).

Information generated in conjunction with the development of a new glass/glass package, with no TPAT backsheet, was considered to explain degradation for some modules made using the package design incorporating a TPAT backsheet. As discussed in the preceding section, broadening and darkening of interconnects, Figure 12, has been found to be an indicator of power losses characterized by lower current due to gross moisture ingress. No darkening and broadening of the interconnects was observed for the dissected module from the array at NREL that lost FF. Smaller (ST10) modules retrieved for nondestructive and destructive testing may have had barely detectable corrosion along the edge of cells but not the darkening and broadening observed for the prototype glass/glass package. Also, the electrical performance change with darkening and broadening of the interconnects is a drop in current rather than an decrease in FF. Therefore, high water vapor ingress and a decrease in Isc does not seem to be the cause of degradation for the subset of modules deployed with a TPAT backsheet. This does not contradict the possibility that a lower degree of water vapor ingress could be responsible for the decreases in FF.

Array data from test sites throughout the country is consistent with and augments the information obtained from individual modules and the NREL array. Figure 19 is a chart of average annual decline in power for 32 module arrays deployed at:

"FSEC" `	- Florida Solar Energy Center, Cocoa, FL
"Wisconsin"	- University of Wisconsin, Madison, Wisconsin
"Gumbo"	- Gumbo Limbo Environmental Education Center & Florida Atlantic University, Boca Raton, Florida
"NREL"	- National Renewable Energy Laboratory, Golden, Colorado
"Austin"	-University of Texas at Austin, Austin, Texas
"SWTDI"	- Southwest Technology Development Institute, Las Cruces, New Mexico

These test site locations represent diverse climates and, as indicated in the figure, two main module configurations, wide and narrow frames, are included in the data. The two module configurations are equally well described as two production timeframes. The average annual decline ranges from slightly negative, an improvement, through minimal changes to significant losses. If there is a climatic component of the changes, it is obscured by other variation. However, a hot humid environment, which would be expected to be the harshest, is not necessary for changes and, in fact, the array showing a small improvement is from an area (Austin) selected for array deployment because of the hot and humid environment.

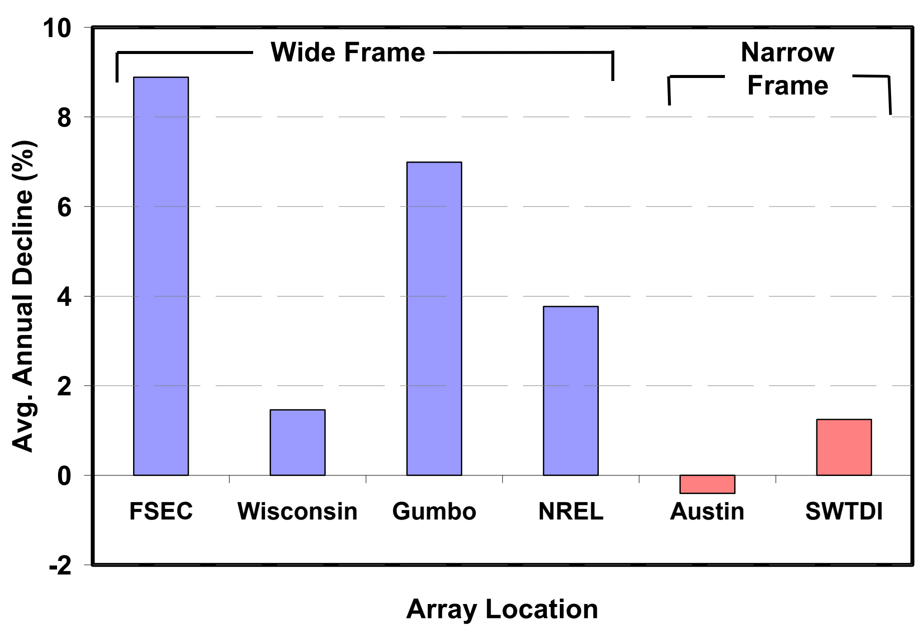


Figure 19. 32 Module Arrays: Average Annual Decline

The presence of any significant loss is best correlated with module configuration or timeframe [17]. This correlation is also consistent with long-term outdoor stability testing for individual modules, Figure 13, where multiple prototype package designs have demonstrated long-term stability. The possible exceptions are the two modules deployed in 1998, which is the same timeframe as the arrays that exhibit losses. Losses are not inherent since multiple past and present arrays have demonstrated stability, a range of array performance from improvement through losses is observed for the timeframe where arrays might show significant losses and within the arrays that show losses there is a range of module performance including no loss. Some failure mechanisms, such as improper use of lay-up tape and dirt buildup for wide frames, have been clearly demonstrated. Other subjective observations imply that additional circuit plate or packaging process variables may have effected long-term stability for pre-production modules produced in the timeframe when wide frames were standard.

Conclusions

Outstanding progress has been made in the initial commercialization of high performance thin film CIS technology. The following are highlights of accomplishments during this subcontract period:

- Executing SSI's process continues to demonstrated predictability of the CIS process.
- Cumulative production for 2002 exceeded 1 MW - about twice the production rate for 2001
- Average laminate efficiency for 2002 is 10.8% with a full width of only 12% of the average.
- Dramatic increases in line yield from improved production protocols and addressing disparate special causes for process variation.
- Line yield increased from about 60% in 2000 to about 85% in 2002.
- NREL confirmed a champion 12.8 percent aperture area conversion efficiency for a large area (3626 cm^2) CIS production module.
- Significant progress was made toward developing a "glass/glass" package that eliminates the TPAT backsheet for decreased cost, simplification of the package and decreased operating temperature
- Field failure mechanisms for prototype modules have been clearly demonstrated. Additional circuit plate or packaging process variables also effected long-term stability for pre-production modules.
- Very promising preliminary results for edge seal developed in collaboration with the new NREL sponsored National Thin-Film PV Module Reliability Team.
- Long-term outdoor stability has been demonstrated at NREL where ~30x30 cm and ~30x120 cm modules with multiple prototype package designs have undergone testing for over fourteen years.

The demonstrated high line yield as the result of process R&D is the major accomplishment. No one major process improvement was responsible for the yield improvements. Dramatic improvements in yield were the result of improving production protocols and addressing disparate special causes for process variation. This major accomplishment supports attractive cost projections for CIS. SSI's thin-film CIS technology is poised to make very significant contributions to DOE/NREL/NCPV long-term goals - higher volume, lower cost commercial products.

Further device and production R&D can lead to higher efficiencies, lower cost, and longer product lifetime. Prerequisites for commitment to large-scale commercialization have been demonstrated at successive levels of CIS production. Remaining R&D challenges are to scale the processes to even larger areas, to reach higher production capacity, to demonstrate in-service durability over longer times, and to advance the fundamental understanding of CIS-based materials and devices with the goal of improvements for future products. SSI's thin-film CIS technology is poised to make very significant contributions to DOE/NREL/NCPV long-term goals - higher volume, lower cost commercial products.

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REPORT DOCUMENTATION PAGE

Form Approved
OMB NO. 0704-0188

1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	March 2004	Annual Technical Report, 24 April 2002–23 April 2003

4. TITLE AND SUBTITLE
Process R&D for CIS-Based Thin-Film PV: Annual Technical Report, 4 April 2002–23 April 2003

5. FUNDING NUMBERS
PVP45001
ZDJ-2-30630-16

6. AUTHOR:
D.E. Tarrant and R.R. Gay

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Shell Solar Industries
4650 Adohr Lane
Camarillo, California 93011-6032

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
National Renewable Energy Laboratory
1617 Cole Blvd.
Golden, CO 80401-3393

10. SPONSORING/MONITORING AGENCY REPORT NUMBER
NREL/SR-520-35684

11. SUPPLEMENTARY NOTES
NREL Technical Monitor: H. S. Ullal

12a. DISTRIBUTION/AVAILABILITY STATEMENT
National Technical Information Service
U.S. Department of Commerce
5285 Port Royal Road
Springfield, VA 22161

12b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 words):* During this subcontract period, predictability of Shell Solar Industries's CIS process was demonstrated by continuously executing the process while increasing throughput. Cumulative production for 2002 exceeded 1 MW - about twice the production rate for 2001. Average laminate efficiency for 2002 is 10.8% with a full width of only 12% of the average. Dramatic increases in line yield were achieved from improved production protocols and by addressing disparate special causes for process variation. Line yield increased from about 60% in 2000 to about 85% in 2002. NREL confirmed a champion 12.8 % aperture-area conversion efficiency for a large-area (3626 cm^2) CIS production module. Field failure mechanisms for prototype modules were clearly demonstrated. Additional circuit-plate or packaging process variables, although not as clearly established, were also found to affect long-term stability for pre-production modules. Significant progress was made toward developing a "glass/glass" package that eliminates the TPAT backsheet for decreased cost, simplification of the package, and decreased operating temperature. Very promising preliminary results were demonstrated for edge seals developed in collaboration with the new NREL-sponsored National Thin-Film PV Module Reliability Team. Long-term outdoor stability has been demonstrated at NREL where ~30x30 cm and ~30x120 cm modules with multiple prototype package designs have undergone testing for over 14 years. The demonstrated high line yield is the major accomplishment. No one major process improvement was responsible for the yield improvements. Judicious application of manufacturing engineering disciplines such as SPC, analysis of variation, and design of experiments led to a clear definition of near-term yield issues. Dramatic improvements in yield were the result of improving production protocols and addressing disparate special causes for process variation. This major accomplishment supports attractive cost projections for CIS. Process R&D at successive levels of CIS production has led to the continued demonstration of the prerequisites for commitment to large-scale commercialization.

14. SUBJECT TERMS: PV; module; device; manufacturers; copper indium diselenide (CIS); thin film; encapsulated module; deposition process; monolithic; large-area reactor;

15. NUMBER OF PAGES

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
Unclassified	Unclassified	Unclassified	UL